



**PCI Express
Development Board** **FREE**

▶ Low jitter and very process tolerant

▶ Small sizes and flexible form factors

▶ Wide output frequency and multiplication ranges

▶ TSMC, UMC, CHRT and Common Platform processes from 180nm to 55nm

The Home
Port

EDA/EDA
Tools

FPGAs/PLDs/CPLDs &
Structured ASICs

Intellectual
Property

Electronic System
Level Design

Special
Topics/Feature
Articles

News

Articles
Online

Tutorials,
White Papers,
etc.

Webcasts

Online
Resources

Software

Tech
Books

Conferences &
Seminars

Vendor &
Organization
Directory

Category: SOCcentral Feature Articles & Columns: Feature Articles:

Sunday, January 06, 2008

Parasitics Move Model Order Reduction into Electronic Design Automation **Featured**

Contributor: EdXact



January 3, 2008 -- Designing a system-on-chip (SOC) and delivering it on time and functional is a challenge and requires a lot of engineering to squeeze the most out of the technology. Today, 40% of design starts are SOCs. In a few years, it will be 70%, according to IBS. Unfortunately, EDA tools are lagging behind advances in fab technology. The sheer complexity of circuit data forces us to apply abstraction and move to higher design levels whenever possible. It's also well known that a small fraction of the design is consistently refusing all the abstraction efforts due to its complexity and variety. We are talking about the analog and mixed-signal parts of an integrated SOC: less than 5% of the SOC transistor count, only 20% of its area, 40% of the overall effort and 50% responsibility for re-spins! In other words, analog circuit design is like chess — just because you know how the pieces move doesn't mean you know how to play, or even win the game.

One of the major problems in analog and mixed-signal design is the need for high accuracy. The distance between the signals and the noise floor is constantly getting smaller. A small change in certain process parameters can turn a working device into garbage. Before re-spinning and losing the market you must perform a sign-off simulation. A vast amount of effort is currently underway in circuit extraction to address all possible and impossible kinds of manufacturing issues.

Generally speaking, interconnect parasitic extraction, which aims at modeling the non-ideal behavior of the copper connections between devices, has become extremely sophisticated. Extraction tools generally use resistors, capacitors and inductors to model Ohmic loss, capacitive charge, capacitive coupling between nets, and coupling magnetically induced from one net into the other. Typical simulation times for analog blocks are measured in minutes. Simulation times for the same blocks with added parasitics are typically measured in hours. Take more than a block and you may wait a week or simply forever.

This problem is not new; netlist crunching has been applied for a couple of years. "Smart filtering" could be applied without real risk, simply because the impact of the parasitics was not that important and could be designed around. This has changed completely in the below 90-nm design space. Here, you absolutely need to take into account cross-coupling and deal with inductance and mutual inductance. Filtering methods are no longer sufficient, and simple algorithms such as TICER, which work well on single uncoupled nets, are out-dated. The strange thing about this is that the problem seems to have been solved in the academic environment through Model Order Reduction (MOR). A large number of different approaches and sub-approaches have been proposed in the literature, but the theories are quite complicated, and very few have found their way into today's EDA tools.

Two reasons for the slow adoption of MOR

First of all, the real engineering world has more constraints, some of which can be ignored in academia. In engineering, we are not working with well-conditioned data, which can be defined as stable and passive. We also need to take into account that after the Model Order Reduction processing, "realizable" networks, with positive, physical values are necessary. Information about circuits are also exchanged in netlist file formats such as Spice, DSPF, SPEF and not in matrix form in the complex frequency domain, as is usually the case in academia. Most of the academic solutions cannot comply with those requirements.

Second, there is the issue of who is responsible for adopting MOR in an EDA company? Those who write the extractors? Their interest is to add even more methods into the extraction algorithms to better capture the influence of physics and anticipate the manufacturing deviations. The generated amount of data is not a problem on the extraction side — disc space is cheap. On the simulation side, the interest is to have accurate data and to keep the runtime of the simulation realistic. Model Order Reduction should, therefore, happen here. But reading in several hundred megabytes, or even gigabytes, is a difficult task. From a simulation point of view, those generating the data (extraction) should have already reduced it on the fly.

This picture is somewhat simplified, but true. It shows that no one takes explicit and

Search for:

in Current Category Site
 Assigned Keywords Text

Go

[Search Tips](#)

Subscribe to
SOCcentral's
**SOC Explorer
Newsletter**
and receive
news,
article,
whitepaper,
and product
updates
bi-weekly.

[Subscribe](#)



Find IP you need

SOCcentral makes it easy by providing listings for more than 300 IP vendors and interfaces to the **ChipEstimate** and **Denali** memory IP search engines.

[Search for IP Now!](#)

ESL Chat
ESL Wishes
for 2008



Grant Martin
Chief Scientist
Tensilica, Inc.
[ESL Chat Archive](#)



Share your ideas.
Ask a question.
Provide an answer.

Participate in an
[SOCcentral Forum](#)

[SOCcentral-Jobs.com](#)
Jobseekers: Check our job listings! Employers: List your jobs for FREE!

dedicated care of the data which needs to be exchanged. This is where EDXACT has found a place. The company's mission is to substantially accelerate existing physical verification flows without the need to change the designer's way of working. Its tools have been able to take away an order of magnitude of the complexity of post-layout verification in different flows, such as RF, analog, mixed-signal and memory design.

By Mathias Silvant

Mathias Silvant is President and CEO of EdXact SA. EdXact SA is focusing on Model Order Reduction and exploitation of information related to the network of parasitics. Mathias graduated with a Dr.-Ing. degree from Hanover University in Germany before starting his career in France. Since then, he has worked at Snaketech, Simplex Solutions and Cadence Design Systems.

[Go to the EdXact website to learn more.](#)

Keywords: SOCcentral, EdXact, parasitics, parasitic extraction, ASIC design, EDA tools, 488/24631 1/3/2008 25 25

[Add a comment or evaluation \(anonymous postings will be deleted\)](#)

Designer's Marketplace

[Add High Fidelity Audio to Your SOC](#)

Use the audio engine found in more cellular phones than any other audio core. See why major companies have picked Tensilica's HiFi 2 Audio Engine to add high-fidelity 24-bit sound to their portable devices.

[5Spice Circuit Simulation](#)

Affordable, easy to use analog circuit simulation. 5Spice provides Spice specific schematic entry, the ability to define and save an unlimited number of analyses and integrated graphing of simulation results. User expandable model Library. Download demo now!

[Rely on Intrinsix for ASIC, SoC & IP Design Solutions](#)

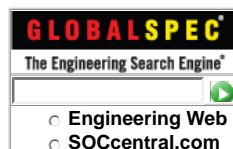
We architect, design and verify high integration devices and systems using digital, analog, mixed-signal and RF ASIC, System-on-Chip (SoC) and FPGA technologies while leveraging our cutting edge IP.

[ChipX Has the Right Slice for You](#)

ChipX offers the broadest portfolio of distinct paths to ASIC for your design with families comprised of technology ranging from 0.6 μ through 0.13 μ supporting designs of up to 10M gates.

[Look to A2e Technologies for Analog Design Services](#)

A2e Technologies excels at analog & RF design. We have a deep understanding of analog and RF design and have completed complex designs for many markets.



[Go back](#)

[Back to Top](#)

Special Topics/Feature Articles

[After DAC 2007](#)
[Design for Manufacturing](#)
[Design for Test](#)
[DSP Functions in FPGAs](#)
[ESL Design](#)
[Floorplanning & Layout](#)
[Formal Verification](#)
[HW/SW Co-Design & Co-Verification](#)
[Logic & Physical Synthesis](#)
[On-Chip Interconnect](#)
[Power Analysis & Optimization](#)
[Reconfigurable Computing](#)
[Signal Integrity](#)
[Structured ASICs & Platform FPGAs](#)
[SystemC](#)
[SystemVerilog](#)
[Transaction Level Modeling \(TLM\)](#)
[Verilog](#)
[VHDL](#)

Designer's Kiosk

Whitepapers & App Notes

[Prototyping Physical Layer IP ASIC with FPGA.](#)

[Processor Core Power Specs: A Cautionary Tale.](#)

Blogs

[Tensilica BlogSpot: All the news from Tensilica.](#)

[Leibson's Law of Disruptive Technology.](#)

Tech Books Store



[Design Recipes for FPGAs](#)
Peter Wilson
New \$45.40
Best \$42.73



[Real World FPGA Design with Verilog](#)
Ken Coffman
New \$80.10
Best \$65.00



[ASIC and FPGA Verification](#)
Richard Munden
New \$56.95
Best \$20.00



[Field-Programmable Logic and Applications. From FPGAs ...](#)
Reiner W. Hartenst...
New \$69.16
Best \$66.39

[Privacy Information](#)

[About SOCcentral.com](#)

[Sponsorship/Advertising Information](#)

[The Home Port](#) [EDA/EDA Tools](#) [FPGAs/PLDs/CPLDs & Structured ASICs](#) [Intellectual Property](#) [Electronic System Level Design](#) [Special Topics/Feature Articles](#)
[News](#) [Articles Online](#) [Tutorials, White Papers, etc.](#) [Webcasts](#) [Online Resources](#) [Software](#) [Conferences & Seminars](#) [Vendor & Organization Directory](#) [About SOCcentral.com](#)

Supporting Organizations



© SOCcentral

Copyright 2003-2007 Tech Pro Communications P.O. Box 1801 Merrimack, NH 03054 603-429-3003
553.488 Execution time: less than 3 second(s)