



PRESS RELEASE

TSMC Selected EdXact Jivaro for 28nm Analog and Mixed-Signal Reference Flow

Grenoble, France and Anaheim, Calif. – June 14, 2010. [EdXact](#), post-layout verification specialist today announced that its netlist reduction software [Jivaro™](#) has been included [in TSMC's Analog/Mixed-Signal \(AMS\) Reference Flow](#) for 28nm analog and mixed-signal circuit design. Analog, mixed-signal, and RF design teams at leading semiconductor companies worldwide now can use Jivaro to efficiently reduce post layout netlist parasitics to speed up their overall simulation time for their 28nm AMS projects.

“We adopted EdXact’s Jivaro tool as an intelligent RC reduction tool to meet the accuracy and compatibility requirements of TSMC’s 28nm AMS Reference Flow 1.0”, said Tom Quan, deputy director of design methodology and service marketing at TSMC.

“Our 28nm collaboration with TSMC in AMS Reference Flow 1.0 is a key milestone to support our mutual customers’ success as they move to this advanced node”, said Mathias Silvant, president and CEO of EdXact. “TSMC's decision to integrate Jivaro as the accurate netlist reduction tool in the industry’s most advanced process flow is a reflection of our tool’s ability to significantly boost design productivity.”

EdXact's Jivaro tool is a netlist reduction platform that enables reduction of layout parasitics in post-layout netlists. Parasitic reduction leads accelerates simulation time and reduces of memory footprint. Combining with accuracy, Jivaro is a productive tool in the design process.

About EdXact

Founded in 2004, EdXact SA focuses on electronic design tools aimed at physical verification tasks. EdXact's innovative model order reduction technology helps accelerate extensive backend verifications in complex IC design cycles. EdXact is headquartered in Grenoble area, France with sales offices in Japan, Korea, Taiwan and India.

For additional information: <http://www.edxact.com>

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Press contact

Chantal Cochini - L'Ops, Conseil & Ingénierie des communications

Tel: +33 6 22 98 03 80

Email: chantal.cochini@lops.fr