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June 14, 2010

TSMC's AMS reference Flow Includes EdXact's Jivaro Netlist Reduction Software



By [Shamila Janakiraman](#) , [TMCnet Contributor](#)

[EdXact](#) a post-layout verification specialist announced that its netlist reduction software Jivaro has been included in TSMC's Analog/Mixed-Signal or AMS Reference Flow for 28 nm analog and mixed-signal circuit design.

Story continues below ↓

Company sources explained that analog, mixed-signal and RF design teams at leading semiconductor companies across the globe will benefit a lot from this inclusion as Jivaro is capable of reducing post layout netlist parasites for hastening overall simulation time for their 28 nm AMS projects.

In a release Tom Quan, deputy director of design methodology and service marketing at TSMC said, "We adopted EdXact's Jivaro tool as an intelligent RC reduction tool to meet the accuracy and compatibility requirements of TSMC's 28nm AMS Reference Flow 1.0."

Mathias Silvant, president and CEO of EdXact further added that the company's 28nm collaboration with TSMC in AMS Reference Flow 1.0 will be beneficial for mutual customers as they move to this advanced node.

"TSMC's decision to integrate Jivaro as the accurate netlist reduction tool in the industry's most advanced process flow is a reflection of our tool's ability to significantly boost design productivity," Silvant added.

According to EdXact its Jivaro tool is a netlist reduction platform which greatly reduces the layout parasitic in post-layout netlists. Also the parasitic reduction leads accelerates simulation time and reduces the memory footprint. As Jivaro is highly accurate it serves customers as an optimized productive tool useful in the design process.

Jivaro 5.0 is a netlist reduction platform which has been enhanced with hierarchical file handling. It has the ability to perform a selective reduction exclusively on a signal path besides being able to reduce parasitic by properties and novelties when reducing for Electro migration or voltage drop.

Jivaro is very useful whenever simulations run long due to an accrued number of parasitics and accuracy of the simulation is most imperative.

France-based EdXact SA specializes on electronic design tools which are required in physical verification tasks. The company model order reduction technology allows fast and extensive backend verifications in complex IC design cycles.

Shamila Janakiraman is a contributing editor for TMCnet. To read more of Shamila's articles, please visit her [columnist page](#).

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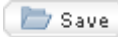
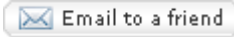
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