

TSMC Selects EdXact Jivaro for 28-nm AMS Reference Flow



June 14, 2010 -- **EdXact** today announced that its netlist reduction software Jivaro has been included in **TSMC's** Analog/ Mixed-Signal (AMS) Reference Flow for 28-nm analog and mixed-signal circuit design. Analog, mixed-signal, and RF design teams at leading semiconductor companies worldwide now can use Jivaro to efficiently reduce post layout netlist parasitics to speed up their overall simulation time for their 28-nm AMS projects.

"We adopted EdXact's Jivaro tool as an intelligent RC reduction tool to meet the accuracy and compatibility requirements of TSMC's 28 nanometer AMS Reference Flow 1.0," said Tom Quan, Deputy Director of Design Methodology and Service Marketing at TSMC.

EdXact's tool is a netlist reduction platform that enables reduction of layout parasitics in post-layout netlists. Parasitic reduction leads accelerates simulation time and reduces of memory footprint.

Go to the [EdXact website](#) to find additional information.



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E-mail [EdXact](#) for more information.

Read more about [EdXact](#) and [TSMC \(Taiwan Semiconductor Manufacturing Company\)](#) on SOCcentral.com

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