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!!!      "It's not a BUG,
/o o\   / it's a FEATURE!"
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\ - /   INDUSTRY GADFLY: "My Cheesy Must See List for DAC 2010"
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by John Cooley

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You might want to print out a hardcopy of this to use as an unofficial guide to the Anaheim DAC exhibit floor next week.

- 1.) With 15 year old PrimeTime faltering for speed in [Wiretap 100114](#), **Magma Tekton** was written explicitly to take on PT's weaknesses. Tekton, like PT, comes in 2 flavors. One for basic STA and one for signoff STA that includes crosstalk, OCV, etc. The difference is Tekton is blindingly faster than PT. For example in one MCMM benchmark of a 1.1 M cell design Tekton took only 28 minutes to complete 21 scenarios doing full crosstalk and OCV (i.e. sign-off) on an 8 CPU machine. PrimeTime-SI took 2 hours per scenario for a total of 42 hours run time. Tekton has built-in SPICE for debugging of critical paths where full SPICE accuracy is needed, plus it supports SDF, SPEF, Verilog, .lib, ILM, SDC, m-tcl, CCS, NLDM models. And unlike other Magma tools embedded in the Magma backend, Rajeev said: "Customers can use Tekton standalone. It's a replacement for PT. This means CDNS users, SNPS users or, if there are any MENT users, them too!!" Tekton (AOCV) is part of the new TSMC Reference Flow 11. Libraries are in TSMC 28 nm and so far 30 different customers are currently evaluating Tekton. (booth 603) Ask for Brandon Bautz. Freebie: lava lamp keychain

Extreme DA GoldTime does both STA & SSTA. "Since last year runtime performance is up 2X, capacity is 30% up, and accuracy is correlated to SPICE. We're 3X faster than PT. Our parametric OCV flow is much faster and easier to use than PrimeTime AOCV for variation analysis." Customers are AMCC, Cisco, Nvidia, PMC-Sierra, STARC, Samsung, ARM. (booth 556) Ask for Ruben Molina. Freebie: soccer squeeze ball

CLK DA Amber Path FX is a fast SPICE-accurate path timing analyzer for delay and statistical variation. Claims "100,000X faster than Monte Carlo SPICE for digital path analysis." It's in TSMC Ref Flow 11. "Let PrimeTime or Cadence ETS find your problem paths. Let Amber Path FX give you your real slack numbers." (booth 373) Ask for Isadore Katz. Freebie: LED keychain

- 2.) It's funny how **Cadence Virtuoso** is still #1 despite what must be \$200 M spent on R&D (collectively) to kill it. To be fair, most of the Virtuoso Killers are playing catch-up to the features that already exist in Virtuoso. For example, rapid prototyping (Magma, Ciranova), device generators (Tanner), IP reuse (Magma), layout migration (Magma, Sagantec), full custom routing (Magma, Pulsic, TeraRoute), and one company is cloning Virtuoso whole (Synopsys). Talk about flattery!

At DAC, Cadence will be yarping up Virtuoso building a DRC/LVS clean Op Amp in minutes, using local optimization to dial in a design, brag about verifying a design across corners, demo yield analysis with new algorithms and distributed job control via ADE XL with 100x speed up. They will also show "Modgens", a device generator that "reduces layout of critical structures by 90%", a constraints-driven device placer, layout constraints checked like DRCs, and auto routing.

The router talk is a rehash of the CSR/VSR they codeveloped with IBM. They cut 35 layout designers down to 5 using CSR/VSR on one project. VIA Tech got a 50% reduction in routing, 25% reduction in area with this same router. I've heard that AMD is using CSR/VSR, too.

Rumor is Cadence is taking on SpringSoft at Marvell, Mediatek, and at the ST library group in Noida. They've added parallel simulation plus fixed basic editing with a smart-attach ruler, improved alignment, synchronous copy in layout, and Project Mercury -- SKILL PCells edited like polygons! (booth 1334) Ask for John Stabenow. Freebie: Poken

Magma Titan ALX is an analog layout accelerator. ALX migrates existing layout, automatically generating DRC-clean layouts using target process technology rules while preserving analog intent. "Combined with Titan ADX, Titan accelerators enables constraint-driven, analog design reuse by producing a new optimized design." There's also a layout-aware schematic design tool called Titan AVP. (booth 602) Ask for Ashutosh Mauskar. Freebie: lava key chains

Solido Variation Designer does variation-aware full custom design. It fixes variation impact on design specifications for PVT corners, local and global random variation and proximity effects. Runs with Virtuoso ADE/Spectre, HSPICE, and Berkeley AFS, speeds variation sim 5x-10x. In TSMC AMC Ref Flow 11. (booth 596) Ask for Patrick Drennan.

Pulsic Unity does custom design automation; which means floorplanning, placement, routing, ECO, SI for high volume designs. "Our customers have used us to tape out at 45 nm and 40 nm (TSMC), and 34 nm (IDM)." OpenAccess. Users Altera, Numonyx, Samsung, Toshiba, Hynix, NEC, Sony

(booth 468) Ask for Mark Waller. Freebie: 5 hour energy shots

Tanner HiPer Silicon v15 -- "Newest release of our full-flow tool suite for design, layout and verification of analog and mixed-signal (A/MS) integrated circuits & MEMS." New waveform analysis, Verilog-A and SPICE views, schematic-driven layout. Users TSMC, Cirrus Logic, Honda, Kionix, Ricoh, Tangent, Honeywell, Raytheon, Proteus, Flir.
(booth 1342) Ask for Nicolas Williams. Freebie: 3-Card Monte trick

Tanner HiPer DevGen is their high performance device generator that "generates current mirror and differential pair structures that are DRC/LVS clean. Maintains layout engineers' freedom over layout."
(booth 1342) Ask for Nicolas Williams. Freebie: 3-Card Monte trick

Ciranova Helix -- "Floorplanning/prototyping/placement for AMS, reads in schematic from Virtuoso/Laker/etc plus iPDK; produces high-quality transistor-level placement and trial-routing which reads back in to Virtuoso/Laker. Multicore/multithread versions used on 50K designs."
(booth 501) Ask for Dave Millman. Freebie: unhappy CDNS employees

Ciranova PyCell Studio creates Python-based PCells for use in any OpenAccess tool. New integrated IDE. Users CSR, TSMC, ST, AMD. Use any open PCell IP in Virtuoso and it gives you a warning message!
(booth 501) Ask for Dave Millman. Freebie: angry CDNS employees

Cybereda ADDS is a analog design debug system for transistor-level designs. "Gives analog designers a 10x productivity breakthrough."
(booth 164) Ask for CK Lee. Freebie: reusable tote bag

SKILLCAD UniVia is a Virtuoso add-on that automatically drops vias of correct size (such as rectangle, small square, big square), proper metal enclosure of via and optimized array pattern (such as 1x3, 2x2) based on the path width/filling area. "Increases wiring speed by 20x."
(booth 782) Ask for Pengwei Qian. No freebie.

ClioSoft VDD -- Visual Design Diff gives engineers the ability to quickly compare two versions of a schematic or layout by graphically highlighting the differences directly in the Cadence Virtuoso design editor. Supports both IC 5.x (CDBA) and IC 6.x (OpenAccess).
(booth 1329) Ask for Michael Henrie. Freebie: poker/blackjack game

Apache Totem is a transistor-level power/ground noise analysis tool used for verification of custom designs. It concurrently analyzes the power noise propagation through power delivery network, substrate network, & package/PCB network. Full-chip dynamic electro-migration
(booth 535) Ask for Aveek Sarkar. Freebie: stuffed panda bears

Sagantec SiFix automatically corrects DRC errors and implements DFM rules in large custom and analog IP. Correction rate is 95-99% resulting in 20x speed-up over manual cleanup. It has full support for Virtuoso database and PDKs. (booth 542) Ask for Coby Zelnik.

GRID SimCheck verifies the accuracy of the electromigration and IR drop simulation results of power grids, signal and clock nets, etc.
(booth 1262) Ask for John Kulusich. Freebie: calculator

3.) **NextOp BugScope** does "full-chip assertion synthesis that leverages RTL and stimulus to automatically generate assertions and functional coverage properties." Users Altera, Entropic, Nvidia, PLX. They claim you "should write 1 assertion for every 10-100 lines of RTL."
(booth 1442) Ask for Yuan Lu. Freebie: glitter wand

Zocalo Zazz does verification that's based on some sort of complicated assertion creation similar to NextOp BugScope. [Unsure.] See both!
(booth 1509) Ask for Khalil Shalish. No freebie.

Cadence Enterprise Verifier (IEV) is a new tool that appears to be a souped up version of IFV and NC-sim slammed together to do a mix of formal and sim stuff "superior to Synopsys Magellan" generating and running traces purely from assertions. Used by ST, Marvell, TI.
(booth 1334) Ask for Tom Anderson. Freebie: plastic cup, Poken

Mentor 0-In Formal does model checking, including automatic checks for common/typical errors, assertion checking for SVA, PSL, OVL, and support for Verilog, System Verilog, VHDL, and mixed language designs. Used by Renesas, Samsung, Stretch, Sun, Brother, Canon, DeShaw, AMD.
(booth 1383) Ask for Mark Eslinger. No freebie.

Jasper JasperGold added "50% improvement in formal proof capacity and performance" plus X-propagation, asynchronous clock designs, protocol certification, low power verification, EasyStart, & ProofGrid Manager. Customers are Nvidia, AMD, HP, Qualcomm, Apple, Broadcom, ARM, Oracle.
(booth 1337) Ask for Alok Sanghavi. Freebie: 1 G flash drive

OneSpin 360 MV this year they added new X-aware formal verification. Works with four state logic 0/1/X/Z. Operational ABV and exhaustive. Users Infineon, Melexis, Bosch, Alcatel-Lucent, Nokia Siemens, Tieto.
(booth 1311) Ask for Michael Siegel. Freebie: puzzle, t-shirt

Avery Insight added "new UPF 2.0 based low power verification flow, DFT analysis at RT-Level, plus deeper sequential analysis using automatic guided search." Also has FSM, scoreboards, X checking.
(booth 1363) Ask for Chris Browy. Freebie: LED flashlight

RealIntent Ascent XV formally determines where X's (unknowns) propagate after a reset state is reached. Their X model removes optimism while managing pessimism at the RTL simulation level.
(booth 722) Ask for Lisa Piper. Freebie: carabiner flashlight

Vennsa OnPoint is a new tool for automatic root cause analysis of failures. It shows "suspects" pointing to the actual bugs with no user direction needed. Works with formal tools & RTL simulators. (booth 250) Ask for Sean Safarpour. Freebie: bottle opener

- 4.) **Apache PowerArtist-XP** added improved modeling for RTL-Gate accuracy, memory power reduction, improved visualization and a seamless flow from PowerArtist-XP to Apache's RedHawk for power grid integrity. They fixed their GUI. Power reduction from 8% - 36% on 50 designs. (booth 535) Ask for Will Ruby. Freebie: stuffed panda bears

Atrenta SpyGlass-Power does power estimation at RTL/Gates with UPF and CPF, identifies new clock and memory gating opportunities at RTL. (booth 744) Ask for Dave Allen. Freebie: solar flashlight

Calypto PowerPro CG automatically reduces power in registers, clock trees, and combinational logic in RTL designs. Calypto PowerPro MG reduces the dynamic and leakage memory power for on-chip memories. (booth 286) Ask for Sumit Roy. No freebie.

Cadence Conformal LP does whiz-bang quality checks on RTL, gates, post-P&R to make sure power saving techniques are implemented right. And the obvious Low Power EC. Ask about creating power intent w/o having to learn one of those pain-in-ass power intent languages! (booth 1334) Ask for Mike Carrell. Freebie: plastic cup, Poken

Nangate Design Optimizer is "the only synthesis tool that can deploy the new TSMC 40 nm LP MegaLibrary and improve speed, power and area between 15-40%. Reduces duration of late stage timing closure by up to 30% with footprint compatible IPO." All employees named "Jens". (booth 1362) Ask for Jens Michelsen. Freebie: fancy pen

Prolific ProPower Elite does block-level, PrimeTime-based, parallel multi-corner, final pass power opto. Gets 25% to 75% leakage power improvement. (booth 561) Ask for Paul de Dood. Freebie: t-shirts

Lib Tech ChipTimer speeds up a gate-level digital design by 2X and reduces gate count by 10% using a new timing optimization technique and some on-fly-fly library generation, enhancing the ASIC library. (booth 580) Ask for Mehmet Cirit. Freebie: Mehmet's undying love

EDXACT Jivaro does netlist reduction for parasitics, RC, but also inductances and others (controlled sources). "Usually used for simulations such as memory timing, analog and mixed-signal blocks, std cell char, power grid analysis." Users Intel, Mediatek, Sony. (booth 1170) Ask for Jeepe Goujon. No freebie.

- 5.) **Mentor CatapultC** -- ANSI C/C++/SystemC/TLM, datapath and control opto. This year they added "full chip synthesis". (Not sure what that is.) Used by ST, Ericsson, Toshiba, Qualcomm, Hitachi, Panasonic, Siemens, TI, Telegent, Pioneer, Fujitsu, Fuji Xerox, Konica Minolta, Thales, Elektrobit, Sanyo, TATA Elxsi, Fraunhofer IIS. CatapultC is in TSMC Ref Flow 11 and again Gary Smith says CatapultC had #1 market share in 2009. (booth 1383) Ask for Thomas Bollaert. Freebie: Espresso

Forte Cynthesizer -- SystemC/TLM, area-power-speed opto plus this year they added CellMath Designer datapath synthesis from Arithmatica. They're also in the TSMC Ref Flow 11 and again Brett says Forte had #1 market share in 2009. Used by Toshiba, Sony, Ricoh, Sanyo, OKI, Fujitsu, NXP, Samsung, NTT, Olympus, Global Unichip, ETRI, and Epson. (booth 750) Ask for Brett Cline. Freebie: caricatures, LED keychain

AutoESL AutoPilot -- ANSI C/C++/SystemC/TLM, area-power-speed opto for both ASIC and FPGA (supports both Xilinx & Altera). Customers are Alcatel-Lucent, Qualcomm, Microsoft, National Instruments, Raytheon, JPL/NASA, Lockheed Martin, Xilinx. (booth 1577) Ask for Atul Sharan. Freebie: toy copter, dancing robot

Cadence C-to-Silicon -- ANSI C/C++/SystemC/TLM, control and datapath, architecture exploration GUI, ECO support, embedded logic synthesis, Wind River to CtoS to Palladium demo. Users Casio, Renesas, TI, ITRI, Fujitsu, Hitachi. (booth 1334) Ask for Mark Warren. Freebie: Poken

- 6.) **Mentor 0-in CDC** has added "hierarchical CDC, merged static and dynamic CDC results, advanced synchronization schemes, support for latch-based designs, integration with UCDB coverage database". Users are Canon, Toshiba, HP, AMD, Broadcom, Fujitsu, Honeywell, Marvell, AMCC, Zoran. (booth 1383) Ask for Harry Foster. No freebie.

RealIntent Meridian CDC has added checks on "reset uncertainty, reset propagation, pseudo constants and encapsulation" and "It can handle 50 M gate designs with more than 300 clock domains in less than 6 hours." Users are Nvidea, Northrop Grumman, Brocade, QLogic, Renesas. (booth 722) Ask for Oren Katzir. Freebie: carabiner flashlight

Atrenta SpyGlass CDC does "analysis to ensure metastability has been correctly isolated, synchronizers are properly used, and that data-coherency, data/enable sequencing and reset assertion/de-assertion issues are avoided." This year they've added a way to "mix blocks". (booth 744) Ask for Shaker Sarwary. Freebie: mind reading trick

Cadence Conformal CDC is at DAC this year, but the CDNS marketing people are being all weird and twitchy about it. Ask them yourself. (booth 1334) Ask for Rich Owen. Freebie: insulated plastic cup

- 7.) **RealIntent PureTime** does "constraints template generation, formal

verification of false and multicycle path exceptions, constraints coverage analysis and SDC equivalency checking. Plus it also does "glitch-aware exception verification" -- whatever that is...? (booth 722) Ask for Shiva Borzin. Freebie: carabiner flashlight

Atrenta SpyGlass Constraints seems a lot like RealIntent PureTime but it can also do multi-mode coverage analysis and EC on two revs of SDC constraints for two revs of the same design. (booth 744) Ask for Ron Craig. Freebie: mind reading trick and solar flashlight

Cadence Conformal Constraint Designer (CCD) does verification just like Conformal LEC, only it makes sure SDCs are complete & correct using structural, functional and EC checks. It works at RTL, gates, pre/post layout and verifies timing exceptions, too. Customizable. (booth 1334) Ask for Mike Carrell. Freebie: Poken

Fishtail Focus merges multiple MCMM constraint files into one single constraint file. "Cutting P&R runtimes in half is huge. It means our customers can keep existing P&R vendor and get a dramatic TAT improvement. It's like spiked gasoline that gives all cars the fuel economy of a Prius." (booth 186) Ask for Ajay Daga. No freebie.

BluePearl is similar Fishtail Focus but it also added something it calls False Path Audit Trail (FPAT) which "tells you why a specific timing exception path is false" plus formal data-stability analysis for multicycle paths plus some CDC stuff. Fujitsu, Xilinx, Philips uses them. (booth 1558) Ask for Prab Varma. Freebie: mug

- 8.) **Mentor Olympus-SoC** has added this year "Project Genesis" which is dataflow graph driven automatic macro placement, routing-aware legalization based on boundary pin analysis and track availability, parallel placement exploration based on multiple configurations (for example if you want to do a placement based on only timing or only congestions or both), fast/accurate pre-CTS timing prediction for accurate floorplanning, intelligent grouping and macro group size reduction. They also added a GDSII chip finishing flow, and distributed timing analysis across multiple cores and machines. **InRoute** is last year's "Project Janus" adding Calibre into Olympus. (booth 1383) Ask for Sudhakar Jilla. Freebie: beer & wine social.

Atoptech Aprisa will be showing SI aware placement for better timing closure, adaptive MCMM analysis for the most efficient memory and CPU usage, and lastly an all new slack-based CTS engine which improves runtimes 3-5x all while giving better quality of results. (booth 1042) Ask for Alpesh Kothari. Freebie: toy rocket

Atoptech Apogee is their new juiced up floorplanner that does timing closure by optimizing inside blocks at the top level without timing re-budgeting between top and block levels. See recent [ESNUG 485 #2](#). (booth 1042) Ask for Daniel Maung. Freebie: toy rocket

Magma Talus this year has a new router, a new timing engine, a new congestion-based RTL synthesis, and dynamic voltage frequency scaling for dynamic power. Users Marvell, Qualcomm, TI, Broadcom, Nokia. (booth 602) Ask for Rob Knoth. Freebie: lava-lamp key chain

Magma Hydra floorplanner provides a full abutment reference flow that delivers hierarchical CTS, abutted pins, constraint budgeting and full chip level design closure. It does best on 1000+ macro designs. Users Toshiba, Nvidia, IDT, Sigma, TI, Vitesse, Nokia. (booth 602) Ask for Mark Baker. Freebie: lava-lamp key chain

Cadence Encounter DFM has variation- and manufacturing-aware design closure, low power, and mixed-signal implementation. "DFM which is over 100x faster than signoff litho analysis. Unlike signoff litho analysis, Encounter DFM has built-in litho pattern knowledge and aggressive filtering, that fixes litho hotspots during routing." (booth 1334) Ask for Manoj Chacko. Freebie: plastic cup, Poken

- 9.) **Oasys RealTime Designer** takes the RTL and floorplan of a full chip to placed gates 10X to 60X faster than Synopsys DC-Graphical can. Supports Verilog, VHDL, System Verilog, multi-mode synthesis, DFT, low power design. Users Juniper Networks, Renesas, STARC, Xilinx. (booth 202) Ask for Paul van Besouw. No freebie.

Tiempo ACC is a synthesis tool for asynchronous design. It's used to design ultra fast and super low (1/5th) power circuits. This year they've added System Verilog. (booth 710) Ask for Nicolas Leblond.

Cadence RTL Compiler Physical (RC-P) added congestion prediction, analysis, fixing, and prevention. Writes a seed placement (DEF) so you get exactly what you signed off, no matter what P&R system you use. Users AMCC, NEC-EL, Zarlink, Ricoh, Global Unichip.

A tool that works with RTL Compiler is **Cadence DFT Architect**. Does "hierarchical silicon test logic insertion with links to True-Time ATPG for predictability through early analysis and verification." Used by Amalfi, NEC, Qualcomm, TI, Hitachi, Fujitsu, Sequans, IBM. (booth 1334) Ask for Rich Owen. Freebie: plastic cup, Poken

- 10.) **Cadence Palladium XP** scales up to 2 B gates, 512 simultaneous users. Users can "hotswap" between SW simulation and HW acceleration modes. Can measure dynamic power use of DUT. Users Nvidia, Nethra, ARM. (booth 1334) Ask for Raj Mathur. Freebie: Poken, insulated cups

Mentor Veloce this year now runs the ARM VSTREAM, which eliminates the need for JTAG HW probe. "Last we heard VSTREAM on Palladium ran

1X the speed [no improvement] of a serial JTAG. VSTREAM on Veloce runs 10X faster than JTAG." (booth 1383) Ask for Jim Kenney.

EVE Zebu does super fast emulation. Now supports TLM 2.0. This is their 10th DAC. Users AMD, ARM, Broadcom, Fujitsu, Konica Minolta, Marvell, NEC, NXP, Qualcomm, Renesas, Sanyo, SanDisk, ST, Toshiba. (booth 510) Ask for Ron Choi. Freebie: reusable tote bag

Dini's Big Virtex-6 FPGA Boards and Big Stratix-4 FPGA Boards. "Our competitors are frantically trying to reverse engineer our products in an attempt to figure out how we do it." Users TI, Qualcomm, Intel. (booth 778) Ask for Mike Dini. No freebie.

Aldec HES does ASIC design emulation, ASIC and FPGA design simulation acceleration, SoC Software/Hardware co-emulation. Added dynamic debugging probes (no need to rerun P&R to change probes), 3rd party hardware (e.g. Dini boards), support for fully automated setup, emulation speed boost up to 10 MHz. Qualcomm uses Aldec HES. (booth 1373) Ask for Igor Tsapenko. Freebie: USB hub, metal pen

Bluespec SVP is a synthesizable virtual platform. It's a "SOC kernel subsystem (including synthesizable models of an ARM processor ISS, memory, peripherals and AMBA interconnect) that runs in EMULATION, in addition to simulation, and provides free ports for customer IP in the form of synthesizable models (before RTL is available) or RTL." (booth 1476) Ask for George Harper. Freebie: wooden ball & cup

- 11.) **ChipVision PowerOpt** analyzes a C/C++/SystemC design for power consumption and then synthesizes the lowest-power architecture to Verilog RTL along with an RTL testbench and UPF/CPF constraints. "PowerOpt produced a design with 40% lower power than the hand-coded design, and 70% lower power than Cadence C-to-Silicon." (booth 1401) Ask for Paul Chaffey. Freebie: 1 G flash drives

Docea Aceplorer does SystemC modeling, simulation and exploration of low power/thermal architectures early in the flow. User ST-Ericsson. (booth 1458) Ask for Ghislain Kaiser. Freebie: funky French candies

NEC CyberWorkBench does C and SystemC synthesis to RTL. Has AXI-AHB bus generator, C-IP libs and Formal verification in C. Until now, tool was only sold in Japan. Users JVC, Hitachi, Panasonic, Renesas. (booth 1641) Ask for Ben Schafer. Freebie: vitamin C candies

Calypto SLEC does Equivalence Checking between C and Verilog RTL; it's a MUST HAVE tool for anyone doing C synthesis for their designs. (booth 286) Ask for Gagan Hasteer. No freebie.

CoFluent Studio -- Generating SystemC from UML allows running a SW SystemC model with a HW SystemC model before C/C++ code is ready for simulation with ISS. (booth 1415) Ask for Vincent Perrier.

Compaan HotSpot -- It parallelizes and translates C-code hotspots to data streaming Kahn Process Networks (KPNs) to utilize highly parallel heterogeneous multicore chip architectures. It offers C code migration. (booth 368) Ask for Bart Kienhuis. No freebie.

Target Compiler lets you use their proprietary nML language to create custom processors. Then they synth it to RTL. Thrown in is a C compiler that lets you run programs on your custom processor. (booth 1376) Ask for John Fox. Freebie: Post-it notes

- 12.) **Cadence Conformal ECO** automates RTL based functional ECOs. Handles pre-mask and post-mask ECOs. "Offers 5X-10X productivity gain over manual ECO." Used by Fujitsu, Broadcom, Teledyne, Cisco, Freescale, (booth 1334) Ask for Bassilios Petrakis. Freebie: Poken

SpringSoft Certitude applies mutation-based testing techniques with static analysis to improve QoR of HDL simulation-based environments. A.K.A. one of the Intelligent Testbenches opined about years ago. (booth 1357) Ask for George Bakewell. Freebie: frisbees

Good olde **Cadence NC-Sim** is now called by Cadence marketing "Incisive Enterprise Simulator (IES)". This year it now supports UVM plus does "multi-core simulation" and I think Verilog AMS. I'm not 100% sure. (booth 1334) Ask for Adam Sherer. Freebie: plastic cup, Poken

Aldec Riviera-PRO does simulation and debugging of System Verilog, Verilog, VHDL, SystemC. OVM and UVM support. Lockheed Martin user. (booth 1373) Ask for Jing Yang. Freebie: USB hub, metal pen

Avery SimCluster does parallel simulation on multicore or networked computers, performance profiling and automatic partitioning. Uses VCS, NC-Sim, Questa as underlying simulator. Speed ups of 5-7X. (booth 1363) Ask for Chris Browy. Freebie: LED flashlight

Cadence Enterprise Manager (IEM) automates. It runs verification CDNS tools on a server farm and collects metrics across these runs. (booth 1334) Ask for Mike Stellfox. Freebie: plastic cup

- 13.) **Sapient Sapient-IC** provides macro level analytics from die size/power estimates to product financials such as profit margins, revenue growth and budget analysis. Competes with **Cadence InCyte & ChipEstimate.com**. (booth 375) Ask for Subash Peddu. Freebie: polo shirts

Tuscany Pinpoint aggregates data from tools as the flow is run, even from multiple vendors and serves web pages that allow designers to compare how metrics are changing as the flow is running. "A designer

can visualize a PrimeTime report against a Magma generated DEF." It "eliminates the need for status reports and even for status meetings." (booth 1584) Ask for Matthew Michels. Freebie: pens

- 14.) **Magma QCP** is Magma's next generation standalone extraction tool. QCP processes up to 50M nets at 4M nets/hour. Its multi-corner extraction adds only about 10% overhead per added corner. Benchmarked 3M nets on a 4 CPU machine: Magma QCP took 45 min, Synopsys Star-RC took 395 min. (booth 602) Ask for Rochelle Drenan. Freebie: lava-lamp key chain

Prolific ProGenesis Elite does 20 nm standard-cell library creation. "Customers hand-drew 45 nm libs in parallel with ProGenesis, plus hand-optimized ProGenesis layouts. ProGenesis produced faster, more power efficient, and denser libs; each by 5% better than hand-drawn." (booth 561) Ask for Paul de Dood. Freebie: t-shirts

Magma SiliconSmart ACE is a IP lib characterization and modeling tool. "Embedded FineSim simulator that leads to unprecedented throughput" (booth 602) Ask for Jerry Zhao. Freebie: lava-lamp key chain

Silicon Frontline R3D & F3D extraction. R3D is the slower Resistive 3D extraction. F3D the Fast 3D extraction. In TSMC Ref Flow 11. "accuracy to 0.001%" (booth 266) Ask for Yuri Feinberg.

Z Circuit ZChar -- "We do memory char really fast - works well with Synopsys HSI. Speedup by 10x and scalable to very large memories." (booth 470) Ask for Ralph Lanham. Freebie: toy guitars

- 15.) **Atrenta SpyGlass-DFT** DSM checks how "at-speed test, low power and test compression impact the design and how to address these issues at early RTL. RTL fault coverage estimation for transition faults correlates to within 2-5% of ATPG results. Users ST, Cisco, STARC. They also have SpyGlass-MBIST which does "RTL memory BIST insertion of proprietary/third-party BIST." -- Note not gate level, RTL level. (booth 744) Ask Kiran Vittal for both. Freebie: solar flashlight

RealIntent Meridian DFT is a new tool for RTL designers to "assure their design is DFT compliant early on. It has smart built-in rules to catch scan-ability issues and does analysis for stuck-at & at-speed tests, plus reports on test/fault coverage"; all at early RTL design! (booth 722) Ask for Rob Thompson. Freebie: carabiner flashlight

Mentor Tessent MemoryBIST does at-speed testing, diagnosis, and repair of embedded memories. It's hierarchical, allowing BIST & self-repair to be added to individual cores as well as at the top level. (booth 1383) Ask for Steve Pateras. Freebie: beer & wine social

Mentor Tessent YieldInsight is a specialized new tool for yield loss from scan test data. It magically uncovers hidden yield limiters. (booth 1383) Ask for Geir Eide. Freebie: beer & wine social

- 16.) **Mentor Calibre PERC** does electrical rule checking, including ESD validation and identification of inappropriate connections between multiple power supplies in mixed-signal ICs. TSMC AMS Ref Flow 11. (booth 1383) Ask for Carey Robertson. Freebie: beer & wine party

Apache PathFinder is a new layout-based tool for full-chip and block-level analysis of ESD (electrostatic discharge) issues in your design. PathFinder is included in TSMC Reference Flow 11.0 for ESD validation. (booth 535) Ask for Aveek Sarkar. Freebie: stuffed panda bears

Magma Quartz -- "Significant runtime improvements and increased runset coverage have resulted in Quartz winning every technical benchmark." Used by IBM, Samsung, Nvidia, TI, Wintegra. In TSMC Ref Flow 11. (booth 602) Ask for Jonathan White. Freebie: lava-lamp key chain

Mentor Calibre nmDRC Auto-Waivers speeds verification of large SoCs by allowing users to attach DRC waivers to their IP datasets so that waived violations will not appear during SoC verification runs. (booth 1383) Ask for Michael White. Freebie: beer & wine party

- 17.) **Cybereda PCSIM** does parallel SPICE simulation. "New company and new SPICE tool that gives 10x or better speed-up vs HSPICE. 5K device PLL simulation ran 29x faster on 8 CPUs vs commercial SPICE tool. Sim of 4.8 days reduced to 4 hours." (booth 164) Ask for CK Lee.

Berkeley AFS -- "Produces identical results to Spectre and HSPICE (guaranteed) 5x-10x faster single-core and up to 50x faster with multi-core parallel operating mode for characterization. AFS handles circuits with up to 10 million elements, and has the only nanometer SPICE accurate device noise analysis." Users Qualcomm, Broadcom, Fujitsu, NXP, Samsung, Sony, LG, NXP, Panasonic, Motorola, Atheros. (booth 1102) Ask for Matthew Parker. Freebie: pens

Magma FineSim -- "Significant performance improvement for transient circuit analysis. Benefits of scalable multi-CPU and a single executable for full SPICE and fast SPICE circuit analysis." (booth 602) Ask for KT Moore. Freebie: lava-lamp key chain

- 18.) **Apache RedHawk 3DIC** does power analysis on 3D multi-die designs, generates CPM that includes device-level current (switching and leakage) and parasitic (diffusion, gate, signal, well) information. (booth 535) Ask for Aveek Sarkar. Freebie: stuffed panda bears

E-System Sphinx 3DEXT is a power and SI cosimulator for IC packaging

and PCB design that allows customers to perform signoff on their designs. Sphinx 3DXT is a 50X faster 3D extractor that can be used for 3D wire bonding, grid arrays or TSV structures. Used by IBM. (booth 261) Ask for Bill Martin. Freebie: pens

Apache Sentinel-PSI performs power and SI analysis for package and PCB designs. It's 3D full-wave engine can analyze power/ground planes and signal nets including cut-outs, meshed planes, power/ground islands, via-pad to trace junctions, and coplanar signal traces. (booth 535) Ask for Aveek Sarkar. Freebie: stuffed panda bears

Not actually a tool. **Atrenta** and **AutoESL** are working with Qualcomm and IMEC on 3D silicon via stacked die designs. It's high-level synthesis and 3D partitioning & floorplanning for multi-die systems. (booth 744) Ask for Mike Gianfagna. Freebie: 3D t-shirt

19.) The **TSMC Pavillion** is yarping up their new TSMC 11.0 Reference Flow. Expect unexpected stuff like Forte Synthesizer and Mentor Catapult C, TSMC's PPA model, 2D/3D multichip design, AMS for 28 nm, Solido, Pyxis, Arteris network-on-chip IP & SW, plus Apache's Pathfinder ESD. (booth 294) Ask for Tom Quan. Freebie: picnic blanket

IC Manage GDP is a design data management system. They added "new security features, new JIRA interface for bug traceability, EDIF to SVG (scalable vector graphics) schematic & layout differencing." Huh? What I do know is they spanked DesignSync in ESNUG [483 #5](#) & [484 #10](#). (booth 550) Ask for Shiv Sikand. Freebie: candy

ClioSoft SOS configuration management & version control integrated with Cadence Virtuoso, SpringSoft Laker, Mentor ICstudio. Added a new web based client interface and command line interface. (booth 1329) Ask for Michael Henrie. Freebie: poker/blackjack game

Mentor Precision Rad-Tolerant does exactly what it says, radiation tolerant FPGA synthesis -- the perfect gift for any developer of spacecraft or weapons avionics that needs to operate in nuked areas! (booth 1383) Ask for Roger Do. Freebie: beer & wine social

Verific sells System Verilog and VHDL parsers to EDA tool developers. Synopsys, Magma, Denali, EVE, Sequence, SpringSoft, Apache uses their parsers along with IBM, Infineon, Nvidia, NXP, Panasonic, Renesas. (booth 348) Ask for Rob Dekker. Freebie: cuddly stuffed giraffe

20.) **Avery VIP** are verification IP models and compliance test suites for PCIe 3.0, USB 3.0, SATA, AXI, AHB. Supports OVM, VMM, Verilog. Users PLX, 3PAR, Lucid, GDA, Snowbush, Analog Bits, Virage, CAST. (booth 1363) Ask for Chris Browy. Freebie: LED flashlight

This year, I have a wait-and-see attitude towards any VIP from **Denali**, **Cadence**, **Synopsys**, and **Virage**. Why? Because these companies have all had recent mergers in VIP which means reorgs and layoffs. The guy who supports that VIP may be gone in 2 months. Needs time to stabilize.

That being said, **Denali** is hosting not one, but TWO DAC parties! (booth 1183) Ask for David Lin. Freebie: tickets to two parties

Anyway, I'll see you at DAC! I'm easy to spot: just look for the tall, fat confused white guy who looks like he shouldn't be there. That's me! :)

- John Cooley
DeepChip.com

Holliston, MA

P.S. And if you found this floor guide useful, please email me. It's a LOT work at a VERY crazy time of year for me to put this together.

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