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EdXact To Enhance Interactive Debugging Capabilities, Hierarchical File Handling and Improved Selectivity Features to Its Post-Layout Analysis Tools at 47th DAC

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*Design Automation Conference, June 14-16, 2010, Anaheim, California, USA-
Booth 1170*

GRENOBLE, France — (BUSINESS WIRE) — May 20, 2010 —

Who/What

EdXact, post-layout verification specialist will showcase the latest tool enhancements of its parasitics reduction and analysis tools. Among the highlights of the tool releases 5.0 of Jivaro™ and 3.2 of Comanche™ are hierarchical file handling, additional features to drive the selectivity options and integrations into different graphical user interfaces in order to facilitate interactive network debugging facilities.

Jivaro 5.0

Version 5.0 of edXact's netlist reduction tool features the ability to group parasitics by property in order to remodel them selectively. The feature is useful for all downstream tools requiring preservation of structure and details on interconnections. Current customers used this feature for the analysis of voltage drop, electromigration, electrostatic discharge and other simulations. Version 5.0 also features major enhancements on EdXact's PathFinder algorithm, an important selectivity feature to accelerate simulation time.

Jivaro is a netlist reduction software platform that enables designers to remodel backannotated design data in a way that allows to substantially speeding up post-layout simulations suffering from an accrued amount of parasitics. The software is compatible with all extraction and simulation tools available today.

Comanche 3.2

Major innovation of Comanche, a parasitics analysis tool, is the possibility to interactively debug parasitics related problems based on a graphical layout view in Cadence's Virtuoso design environment, or in SpringSoft's Laker design environment. Comanche 3.2 benefits also from a new toolbox which generates helpful statistics on a net-per-net basis and allows to compare two different extracted netlists.

Comanche, dedicated to problems related to interconnect has been boosted by an order of magnitude for very large nets. The tool reads netlists in standard formats (DSPF, SPEF) and analyzes extremely quickly and accurately parasitic networks. A typical application of Comanche is the determination of the compliance with ESD design rules. Comanche can be run in batch mode for large post-layout verification runs. It can also be used in interactive mode. For interactive mode, tight integrations into major design environments have been developed.

When/Where:

Product Demonstrations

0900-1800 Monday June 14
 0900-1800 Tuesday June 15
 0900-1800 Wednesday June 16
 European EDAVillage: booth # 1170

Information and Registration

To schedule a meeting with EdXact, please email [Email Contact](#) or call +33 476 668 980.

For more information about EdXact, please visit <http://www.edxact.com>.

About EdXact

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 Altium Designer Release 10, making electronics design data management an easy reality.
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- RTL to Silicon
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DAC #535

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