

## NEW WHITE PAPERS

- [Synopsis White Paper: Understanding the real cost of prototyping hardware](#)

Synopsis

- [The PSP Model in RF CMOS Design](#)

Fujitsu  
Microelectronics  
America, Inc.[More White Papers...](#)

## BLOGS

## Verification Vertigo

[Is DAC dying?](#)

People came to DAC this year wanting to be depressed. The industry is in bad shape, the organizing committee made mistakes in...

## Koby's Kaos

[Global Warming for Brains 2 \(the Twitter Variant\)](#)

I hate having to recant. This started out a couple of years ago in my editor's notes in the FPGA Developer newsletter (now...

## Tuning into Jim

[Doug at DAC](#)

One of the less recognized aspects of the Design Automation Conference is the Pavilion Panels program that takes place on the...

## JB's Circuit

[DAC Tuesday - From the Denali Party Floor](#)

EDA's bloggers await the readers vote for the best! And the

## ARTICLE

[\[ Printer Friendly \]](#)**Max's Chips and Dips: Don't Forget the Little Guys at DAC**

In which I present some suggestions (in no particular order) for folks you should take the time to visit while meandering your way around the exhibit halls...

By Clive (Max) Maxfield



It's that time of the year again! DAC 2009 is in full swing as I pen these words. As usual, the "Big Boys" of EDA are firing barrage after barrage of marketing propaganda, and press releases are flying around like confetti. But what about the "Little Guys" ... who will speak on their behalf? Yes! You've guessed it ... yours truly will take the initiative.

Now you must understand that the following is not an exhaustive list ... a whole bunch of smaller companies and newbies (first time attendees) are present at this year's festivities... the following offers just a few suggestions (in no particular order) for folks you should take the time to visit while meandering your way around the exhibit halls.

**Warthman Associates:** [www.warthman.com](http://www.warthman.com), Booth 4205

Actually, let's start with Warthman Associates, because I once saw an amazing presentation by Forrest Warthman showing pictures of the insides of silicon chips and comparing them to bird's eye photographs of cities, bridges, interstate highways... and all sorts of things. It's hard to describe, but he received a standing ovation.

But we digress... Warthman Associates are technical writers specializing in the hardware and software of microprocessors, graphics processors, embedded processors, networking, and semiconductor-design tools. All of their writers have BS or MS degrees and many years of industry experience in electrical engineering and computer science. They say that they write and edit engineering specifications, reference manuals, data sheets, and user guides of the highest quality.

In addition to examples of their technical writing and personal consultations on how to solve documentation needs, they also have a presentation on how to write a maintainable engineering specification.

**XJTAG:** [www.xjtag.com](http://www.xjtag.com), Booth 3954

XJTAG sell a range of boundary scan (IEEE 1149.1) software and hardware products that can test both JTAG and non-JTAG devices that will enable you to debug, test and program electronics circuits quickly and easily. The folks at XTAG say that their tools are ideal for developers and test engineers who need to detect faults in circuits containing FPGAs, CPLDs, DSPs or microprocessors. They also say that you should stop by and say "Hi" to Lorena (from Ireland) and Jessica (from London) who have flown in especially to be on the XJTAG booth. Also that you can enter the world famous XJTAG "Crack the Safe" competition and see if you can create the winning combination to open the safe (yes we have the safe on the booth) and win an iPod or SatNav.

**Achilles Test:** [www.achillestest.com](http://www.achillestest.com), Booth #912

Drop by to the Achilles Test booth to see how their customers are using project heatmaps and other innovative realtime dashboards to understand overall project health and to pinpoint problem areas. They say that their Achilles DVNotebook allows engineering teams to organize and analyze all of the relevant information in a design project: it affords them real-time status and instant access to results from any web browser.

## SYSTEM-LEVEL DESIGN ONLINE COMMUNITY

**System-Level Design** COMMUNITY

This brand new online community is the destination for embedded system design, verification and debugging of system-on-chip (SoC) designs. Site includes news, articles, white papers, videos, blogs, polls, ask the expert and more. [VISIT TODAY!](#)

Sponsored by:

## LOW-POWER DESIGN ONLINE COMMUNITY

**Low-Power Design** COMMUNITY

Low-Power Design is the ultimate resource for engineers and system architects looking for ways to reduce power consumption, spot new trends and to communicate with their peers. [VISIT TODAY!](#)

Sponsored by:

## FEATURED VIDEOS/PODCASTS

[John Blyler interview's Max Domeika from Intel about embedded multicore development](#)

[more videos...](#)

## NEWSLETTERS

[Chip Designer](#)[Chip Designer Plus](#)[PLD Designer](#)[IP Designer & Integrator](#)[SUBSCRIBE NOW](#)

## IP SEARCH

ChipEstimate.com

Find detailed information about thousands of commercially available IP blocks from more than 230 suppliers

[Go](#) [Advanced Search](#)

winner is ... Karen Bartelson! Congrats! Karen sets...

#### POLL

Where will the device design growth be in ten years?

- Multicore
- Programmable
- Wireless
- Low-Power
- IP
- New Technology

Vote!

[View Results](#)

**GateRocket:** [www.gaterocket.com](http://www.gaterocket.com), Booth 3550

Now I personally love this concept. GateRocket offers a verification and debug solution for advanced FPGAs called the RocketDrive. This enables users to verify and debug advanced FPGA designs faster and with higher quality for greatly improved time to market, and realize more reliable and predictable results.

It's actually difficult to explain what this does in just a few words, but bounce over to their booth and ask for a demo and I am sure you will be impressed.

**Sequence Design:** [www.sequencedesign.com](http://www.sequencedesign.com), Booth 3455

The folks at Sequence bill themselves as "Low-power RTL Design Experts." At DAC they will be announcing PowerArtist-XP, which they say is the first and most comprehensive analysis-driven, automatic RTL power-reduction technology within a completely integrated environment. IP and SoC RTL designers, without becoming power experts, can analyze, visualize and reduce power by 10-60% or more within minutes on multi-million instances, with 50% fewer RTL edits, and productivity gains of 10X at a minimum.

**Agnisys, Inc:** <http://agnisys.US>, Booth 4064

Agnisys say that they are one of the "Little Guys" exhibiting at DAC for the first time, and they would love to demo their tools. They say that IDesignSpec enables you to embed registers in your functional specification and extract all derived view from it, saving you time and improving quality. IVerifySpec manages functional requirements, verification plans and results in an intuitive document based editor, which helps you see the precise progress of the verification effort.

**Chipworks:** [www.chipworks.com](http://www.chipworks.com), Booth #4203

First time exhibitor to DAC, Chipworks (a world leader in reverse engineering and patent infringement analysis) is demonstrating reverse engineering in ICWorks using real examples from a Texas Instruments RF Transceiver and an SRAM Macro from Intel's 45nm Atom Microprocessor.

**Desaut Inc:** [www.desaut.com](http://www.desaut.com), Booth 1207

The folks at Desaut have developed a macro language, MacroRTL, that can automate Verilog coding. One line of MacroRTL code that defines a logic object can be expanded into many lines of Verilog codes that define the logic and declare the signals in the logic. At this year's DAC they are announcing two new products: MacroRTL Basic and MacroRTL Pro.

They say that MacroRTL Basic is a very useful subset of MacroRTL. It is aggressively priced to attract people to start using MacroRTL. A trial version is free. The only limitation is the number of lines of source codes. A perpetual license of MacroRTL Basic is priced at USD 20.00. Also that they are re-pricing MacroRTL during DAC. It will be USD 200.00 for a perpetual license. A free trial version also will be available for 3 months.

MacroRTL Pro is the new high end product they will be offering. It is MacroRTL plus a Verilog Design Library. The Design Library includes many design objects used frequently, such as priority encoders, register files, synchronous FIFOs, round-robin arbiters, etc. One line of MacroRTL command can personalize the object. The command be expanded into tens to hundreds of lines of Verilog codes. The user enjoys the reduction of work and bugs, and the benefits of correct-by-construction and designing at a higher level of abstraction.

**DOCEA Power:** [www.doceapower.com](http://www.doceapower.com), Booth 3143N

If you're interested in power and thermal analysis at the system level, then check out the folks at DOCEA Power. They say that their platform ACEplorer is the first ESL software that allows designers to model, simulate, and optimize dynamic power and thermal behaviour of whole complex systems whether on-board or on-chip, including hundreds of blocks. They also say that only a few seconds to minutes are sufficient for performing dynamic electro-thermal simulation including early analysis of risks that threaten reliability such as IR-Drop or thermal runaway.

**EDXACT:** [www.edxact.com](http://www.edxact.com), Booth 3765

The folks at EDXACT say that they accelerate post-layout verification flows suffering from a paramount number of parasitic devices. The clever thing is that you do not need to jump on a new simulation tool, but rather optimize your existing tooling. They have two tool families: Jivaro and Comanche.

Jivaro provides accurate netlist reduction and remodeling using

#### RESOURCE CATALOGS AND GUIDES

- [Chip Design Resource Catalog](#)
- [Chip Design Buyers' Guide](#)
- [Interoperability Guides](#)
  - [Cadence and Third-Party Solutions Guide](#)
  - [Mentor Graphics Questa Vanguard Program](#)
  - [OCP IP Member Guide](#)
  - [Synopsys Interoperability Guide](#)
- [IP Solutions Resource Catalog](#)
- [Valuable Resources](#)
  - [AdvancedTCA](#)
  - [DSP](#)
  - [FPGA and CPLD Resource Catalog](#)
  - [MIPS® Embedded Resource Catalog](#)
  - [Multicore](#)
  - [PCI Express](#)
- [Visit Dot.Org](#)
  - [Model OCP Interfaces in SystemC](#)
  - [Industry Standards Should Facilitate Multicore Adoption](#)
  - [GSA Mixed-Signal/RF Subcommittee Is Facilitating an Analog Ecosystem](#)

[Click here for more...](#)

#### COMMENTARY

- [Power Trump's Time-to-Market as Main Driver](#)
- [Messing with Microcontrollers](#)
- [Too Much of a Good Thing?](#)
- [Synthesis Needs to Change to Serve Modern Chip Design](#)

[More commentary...](#)

mathematical model order reduction techniques. The result is to speed up circuit simulation with layout parasitics without changing the simulator.

Comanche is a netlist parasitics analyzer. This allows you to quickly figure out parasitics-related problems avoiding the need to perform lengthy circuit simulations.

---

**Enterpoint:** [www.enterpoint.co.uk](http://www.enterpoint.co.uk), Booth 4207

A first time exhibitors at DAC, the folks at Enterpoint are launching a new product family for the ASIC Prototyping and High Performance Computing markets. The first of the Merrick family, Merrick1, launches with 101 FPGAs on board consisting of a 10x10 array of Xilinx Spartan-3A DSP XC3SD3400A and a Virtex-5 as an external world connectivity and programming control.

The board has 1600 general I/O connecting the FPGA array directly to the outside world giving an I/O data throughput capability of up to 400 gigabit/s. It also has 2 gigabit Ethernet interfaces, and it also has 8 sets of TX/RX running at up to 3.75 GBit/s each direction. The latter is for board stacking for larger arrays but can be used more generally.

---

**E-System Design:** [www.e-systemdesign.com](http://www.e-systemdesign.com), Booth 508

Another new company exhibiting at DAC for the first time this year is E-System Design. They are announcing their first product, Sphinx, a Signal and Power Integrity Co-Simulator for IC packaging, printed circuit board, and system design. They say that Sphinx uses a new methodology (Multi-layer Finite Difference Method (M-FDM)) and IP exclusively licensed from Georgia Tech to very accurately model critical paths up to complete packages, printed circuit boards and systems.

Because Sphinx can handle much larger complexities than full wave simulators, and is more accurate than current fast EM solvers, it is the industry's first viable sign-off tool for package, PCB and system designs.

---

**EVE:** [www.eve-team.com](http://www.eve-team.com), Booth 908

The folks at EVE aren't a first-timer at DAC, and if they manage to keep on being successful it may not be long before they no longer qualify as being one of the "Little Guys". As you are doubtless aware, EVE's ZeBu-Server is a scalable emulation system, expandable to one-billion ASIC gates, suitable for all SoC verification needs across the entire development cycle, from hardware verification, hardware/software integration to embedded software validation.

At DAC this year, EVE say that they are announcing that they beat their largest competitors at breaking the billion-gate barrier.

---

**Fidus Systems:** [www.fidus.com](http://www.fidus.com), Booth 4204

Another first timer at this year's DAC is Canadian company Fidus Systems who specialize in high speed electronic product development for a wide range of clients in different industries. They say that Fidus has world-class capabilities in Signal Integrity and PCB Layout (amongst lots of other stuff).

---

**Forte Design Systems:** [www.ForteDS.com](http://www.ForteDS.com), Booth 1225

Forte's Cynthesizer creates optimized RTL code from high-level standardized SystemC for control and datapath designs. At DAC they will be demonstrating new features of Cynthesizer, including automated design partitioning, automated generation of verified interface IP, accurate simulation/modeling capabilities not available in ANS-C++, TLM synthesis, SystemC 2.2 support, and REAL success stories.

---

**ATopTech:** [www.atoptech.com](http://www.atoptech.com), Booth #3167

Atoptech will be highlighting their new product, Apogee, that they announced at this year's DAC along with their flagship product Aprisa. Apogee is a hierarchical physical design solution, said to be the first in the industry to seamlessly integrate all the critical hierarchical design functions with a market-leading block-level implementation tool in a single environment.

---

**ClioSoftBooth:** [www.cliosoft.com](http://www.cliosoft.com), Booth 3651

The folks at ClioSoft say that their SOS Design Data Collaboration Platform enables efficient management of design data from concept through tape-out and improves global team productivity. Built to handle the unique demands of designers, the SOS platform gives design teams the freedom and flexibility to choose the way they work, share and collaborate. At DAC they will be demoing SOS with custom-engineered adaptors that seamlessly integrate SOS with leading design flows:

Cadence Virtuoso Custom IC, Synopsys Custom Designer, Mentor ICStudio, and SpringSoft Laker. In addition, ClioSoft's innovative Universal DM Adaptor technology "future proofs" your DM needs by ensuring that data from any flow can be meaningfully managed.

---

**Pyxis Technology:** [www.pyxistech.com](http://www.pyxistech.com), Various booths (see notes) Pyxis will be demonstrating its new NexusRoute-HPC custom digital and analog router for the first time. They say that NexusRoute-HPC is an OpenAccess-based plug-and-play routing technology that, when coupled with today's leading physical layout editors, enables groundbreaking design flow productivity for custom digital and analog designs. NexusRoute-HPC reduces design time from weeks to hours by providing highly automated hierarchical custom routing and chip assembly with an integrated "what-if" analysis capability.

NexusRoute-HPC is being demonstrated in various booths at DAC -- the SpringSoft Custom IC Design Automation showcase, the Synopsys Standards Booth, the TSMC Open Innovation Platform Forum, and the Si2 booth.

---

**Satin IP:** [www.satin-ip.com](http://www.satin-ip.com), Booth #2124

Based in Montpellier, France, the folks from Satin IP have just announced a collaborative program with Toppan Photomasks and Xyalis to improve design for mask manufacturing. At DAC, they are demonstrating a design environment prototype that offers a first set of design rules with monitoring capabilities and links to mask data preparation tools.

---

**Solido Design Automation:** [www.solidodesign.com](http://www.solidodesign.com), Booth #3060

The guys and gals at Solido Will be demonstrating, in a suite-only area, their newly announced Variation Designer solution along with the newest application, Solve Well Proximity, that they say analyzes and solves well proximity effect problems that become major concerns at 90 nm and below. The new Solve Well Proximity application allows semiconductor designers to avoid heuristics-based conservative guard-banding or multiple iterations between circuit and layout.

---

**Synfora:** [www.synfora.com](http://www.synfora.com), Booth #1440

The chaps and chappesses at Synfora Will be demonstrating in a suite only area their newly announced PICO Extreme Power, along with their other Algorithmic Synthesis solutions PICO Extreme and PICO Extreme FPGA. PICO Extreme Power was announced in June 2009 and has significantly reduced power up to 50% on several designs. They will also be discussing the Top Ten Guidelines for Implementing ESL Synthesis.

---

**Tuscany Design Automation:** [www.tuscanyda.com](http://www.tuscanyda.com), Booth #3955

The folks at Tuscany specialize in structured placement and visualization solutions for integrated circuit (IC) design. They focus on providing ease of collaboration, access, and implementation to design teams and managers. At DAC they will be highlighting two new solutions: (1) the industry's first web-enabled visualization and control software for physical design data and (2) a structured design accelerator.

---

**Berkeley Design Automation:** [www.berkeley-da.com](http://www.berkeley-da.com), Booth #1620

This year at DAC, those clever folks at Berkeley Design Automation will be highlighting how their AFS Platform enables AMS/RF design teams to verify what would otherwise require numerous simulators, achieve 2x higher verification efficiency, and signoff with what they say is the industry's only true SPICE accurate device noise analysis. They say that their new AFS Nano delivers foundry-certified true SPICE accuracy, 5x-10x faster for blocks with up to 5K elements for only \$1,900 for a 1-year time-based license.

---

**Methodics LLC:** [www.methodics-eda.com](http://www.methodics-eda.com), Booth 1924

The folks at Methodics specialize in developing design data management (DM) tools for ICs. At this year's DAC they are showing what they say is the industry's first tool suite for global IC design collaboration. They say that their new tools allow hardware designers to make use of advanced software-style tools and methodologies, such as SCM (software configuration management), revision control, and design review, all integrated seamlessly into the IC design environment.

They also say (rather humbly I might add) that "Providing standard SCM functionality on an advanced modular platform that enables hardware design methodologies in a version-controlled context, the new Methodics solution represents a revolutionary approach to global design

collaboration."

---

**R3 Logic:** [www.r3logic.com](http://www.r3logic.com), Booth 813

Another first time exhibitor at DAC, R3 Logic claim to be "The premier 3D EDA company." They say that they've been in this field for over 14 years as it has grown from a research curiosity to the hottest topic in the semiconductor world.

It's certainly true that 3D integration with Thru-Silicon Vias (TSV's), with or without Silicon interposers, is emerging as the solution to the RLC limitations of wirebonded SiP's. 3D-integrated packages permit higher speed, higher bandwidth memory accesses, and tight coupling of analog and digital functions in mixed signal systems.

R3 Logic's product, R3Integrator is said to be the first tool of its class with true 3D-awareness, created specifically for heterogeneous IP integration in stacked die configurations. Compatible with industry standards data formats such as OpenAccess, LEF/DEF, Verilog, GDSII and Gerber, R3Integrator can work with models of fully finished die, adding TSV pads, creating interposer layers and routing from the die to the interposer TSV's. It can also be used to add TSV's within a circuit die, connecting to another circuit die or to the package substrate.

---

**Lynguent, Inc:** [www.lynguent.com](http://www.lynguent.com), Booth 4060

The guys and gals at Lynguent say that they are revolutionizing analog and mixed signal electronic design productivity with their flagship product, the ModLyng Integrated Modeling Environment (IME). ModLyng IME is a graphical modeling environment that enables the drag and drop composition of behavioral models and the design of tests through the use of model building blocks. Models are automatically generated to work in simulator-specific dialects of Verilog-A, Verilog-AMS, and VHDL-AMS. Modlyng IME works within a designer's existing design flow and supports "push button" simulation of test runs.

---

**Arteris:** [www.arteris.com](http://www.arteris.com), Booth 1100 (the Chip Estimate Booth)

The folks from Arteris are to be found in the Chip Estimate booth as part of CE's IP Talks series. Arteris will show their network-on-chip (NoC) solution for on-chip interconnect. New at this year's DAC is P-NoC, which is used for integrating peripheral (the P) IP and functionality into a NoC.

---

**Tela Innovations:** [www.tela-inc.com](http://www.tela-inc.com), Booth 710

Tela say that they are showing the latest enhancements in their design and manufacturing co-optimization technology offering. They have two sets of technology - one aimed at power reduction and one at reducing area - that work closely with the underlying process to help designers address those issues in concert with the physics of the process. As you may recall, Tela bought Blaze DFM earlier this year and they continue to work on that technology and with TSMC on the PowerTrim service that the foundry offers based on Tela's gate length CD biasing technique. Similarly, on the area side, Tela's one-dimensional, straight line layout structures help reduce die size and will also be offered as a service by TSMC (Area Trim).

---

**Oasys Design Systems:** [www.oasys-ds.com](http://www.oasys-ds.com), Booth 3061

Oasys Design Systems offers RealTime Designer, a "Chip Synthesis," product category that reinvents RTL synthesis for chips beyond 20-million gates. The Oasys folks say that their Chip Synthesis technology can synthesize an entire design from RTL to placed gates in a single bite, and do it in a fraction of the time. They also say that Leading-edge semiconductor companies worldwide have started using Oasys.

---

**Verific Design Automation:** [www.verific.com](http://www.verific.com), Booth 3545

The chaps and chappesses at Verific develop SystemVerilog and VHDL front ends for EDA tools used to parse, analyze, and elaborate IEEE standard SystemVerilog and VHDL. They say that Xilinx just released ISE Design Suite 11 fully integrated with the Verific front end. Also, check out Verific's new Static Timing Analysis component. It is ready and Verific is actively looking for beta customers.

---

Last but certainly not least, there are quite a few small companies who (for one reason or another) don't have their own booth at DAC. But this doesn't mean that they aren't at DAC wandering around seeing what there is to be seen. So if you are interested in any of these companies, you could visit their websites and contact them and try to arrange a meeting somewhere at DAC:

---

**Gemini:** [www.gemini-da.com](http://www.gemini-da.com). Starting to get some traction with their

multi-threaded SPICE accurate analog/mixed signal simulator.

**Open-Silicon:** [www.open-silicon.com](http://www.open-silicon.com). Recently announced MAX products to support their customers need for lower power and higher performance designs.

**Palmchip:** [www.palmchip.com](http://www.palmchip.com). Specialists in SoC platforms and IP cores for mobile devices, embedded software and software applications, and as one company's effort to help kick-start the economy, Palmchip is providing a wide range of free IP cores and one-time use of a free design platform.

**Sidense:** [www.sidense.com](http://www.sidense.com). The guys and gals at Sidense specialize in OTP memory products and 1T fuse technology

**Zocalo Tech:** [www.zocalo-tech.com](http://www.zocalo-tech.com). Zocalo Tech's Zazz (try saying that ten times quickly) enables cost effective use of designer-provided assertion checkers by automating the tedious and error prone tasks of using checker libraries.

---

Well, all I can say is "Phew!" There's enough here to keep us all busy for a very long time. Until next time, have a good one!

-----

Clive (Max) Maxfield is the author and co author of a number of books, including [Bebop to the Boolean Boogie \(An Unconventional Guide to Electronics\)](#), [The Design Warrior's Guide to FPGAs](#), and [How Computers Do Math](#); featuring the pedagogical and phantasmagorical virtual DIY Calculator. In addition to being a hero, trendsetter, and leader of fashion, Max is widely regarded as being an expert in all aspects of computing and electronics (at least by his mother). Max was once referred to as "an industry notable" and a "semiconductor design expert" by someone famous who wasn't prompted, coerced, or remunerated in any way.

.....

[HOME](#) | [ABOUT](#) | [SUBSCRIBE](#) | [ADVERTISE](#) | [CONTACT US](#) | [PRIVACY STATEMENT](#)

All materials on this site Copyright © 2009 Extension Media LLC. All rights reserved.