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edXact to release enhanced EDA tools at DAC

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07/15/2009 10:25 AM



PARIS — At the approach of the 46th Design Automation Conference in San Francisco, Calif., edXact SA, French EDA startup specializing in parametric extraction and physical verification, announced it will launch version 3.1 of its Comanche parasitic rule checking analyzer and version 4.3 of its Jivaro simulation acceleration software.

edXact said its Comanche 3.1 parasitic rule checking analyzer now features an application programming interface that makes it possible to program and integrate Comanche in automated mixed-signal and digital flows using scripting languages such as TCL, Perl and Python.

Among other features, edXact highlighted the faster calculation of effective resistance, the user-friendly visualization of most resistive path detection so as to choose source-to-target path analysis as well as the integration into the Cadence Virtuoso environment with support of the Open Access-based versions 6.x.

"With these new capabilities, Comanche cuts the simulation cycles even shorter," claimed Mathias Silvant, edXact's president and CEO. For instance, he continued, "Comanche has been used in a production flow in order to determine the effective resistance of a full R network. While the original simulation-based flow took several hours, Comanche generated the same results in minutes."

Moving to its Jivaro 4.3 simulation acceleration software, edXact said innovations include the compatibility with electromigration (EM) analysis tools, an extended support for RC subnets modeling large power nets and substrate, as well as an improved support of highly hierarchical netlists.

"Electromigration is becoming a major design problem due to increased current densities related to IC down-scaling," commented Silvant. "In order to provide reliable electromigration-robust IC layout we have implemented a Jivaro reduction compliant with EM analysis tools. Jivaro is now able to adjust differentiated parasitic reduction handling to vias and different metal layers."

At DAC, edXact said it will also showcase the upcoming path finder feature as a major upgrade of the upcoming Jivaro 5.0 generation of its netlist reduction tools. The Jivaro path finder algorithm is said to allow users to select a complete path from source to target, including nets and components, and apply to that path a reduction rate that can be different from the rest of the circuit enabling easy optimization of post-layout verification flow, the EDA firm

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Around EE Times Europe



Chaos upsets IC supplier rankings

Seventeen of the top 20 semiconductor companies changed positions in the first quarter, according to market research firm IC Insights.



The Silicon 60 version 8.0

The EE Times 60 Emerging Startups list, first published in April 2004, has been updated to version 8.0 to reflect the latest corporate, commercial, technology and market

conditions.

Which one of the following IC-related product categories will do best as the electronics industry emerges from recession?

- 1) IP and cores
- 2) Analog, mixed-signal, MEMS ICs
- 3) Processors and FPGAs
- 4) Memories
- 5) RF, microwave and optical
- 6) Displays and lighting

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