

edXact Releases Electromigration-Aware Version of Jivaro and Production-Proven Version of Comanche. To Preview Jivaro 5.0 at DAC

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GRENOBLE, France - (Business Wire) [edXact](#) SA, layout verification specialist, today announced that it will release versions 4.3 of its flagship simulation acceleration software Jivaro™ and version 3.1 of its parasitic rule checking analyzer Comanche™ at [DAC](#). edXact also will showcase the new path finder feature as a major upgrade of the upcoming Jivaro 5.0 generation of its netlist reduction tools. Jivaro 4.3, preview Jivaro 5.0 and Comanche 3.1 will be demonstrated in Booth # 3765 at this year's Design Automation Conference, being held in San Francisco, July 26-31.

Major innovations of Jivaro 4.3 include compatibility with EM analysis tools, extended support for RC subnets modelling large power nets and substrate, improved support of highly hierarchical netlists. With the path finder feature, next Jivaro 5.0 tools will enable easier optimization of post-layout verification flow.

New features of Comanche 3.1 include availability of an application programmable interface (API), faster calculation of effective resistance, visualization of the most resistive part of a path allowing users to pinpoint problems with the interconnections very quickly.

Both edXact's tools are tightly integrated into the Open Access based Cadence Virtuoso environment.

Jivaro: What's New ?

« Electromigration is becoming a major design problem due to increased current densities related to IC down-scaling. » said Mathias Silvant, edXact's president and CEO. « In order to provide reliable electromigration-robust IC layout we have implemented a Jivaro reduction compliant with EM analysis tools. Jivaro is now able to adjust differentiated parasitic reduction handling to vias and different metal layers. We have been working very closely with our customers in order to enable those features and make the Jivaro technology available for those flows. »

Jivaro 4.3 tools have substantially improved to support RC subnets of large power nets and substrate and highly hierarchical netlists in order to let users address multi-billion-parasitics netlists.

Tightly integrated into the Cadence Virtuoso 6.x environment, Jivaro 4.3 supports Open Access.

Jivaro: What's Next?

EdXact will furthermore preview upcoming Jivaro path finder major feature to accelerate simulation time. The Jivaro path finder algorithm allows users to select a complete path from source to target, including nets and components, and apply to that path a reduction rate that can be different from the rest of the circuit enabling easy optimization of post-layout verification flow.

Comanche 3.1: What's Up?

Edxact will also introduce a production-proven version of Comanche, its parasitic rule checking analyzer.

Four major advances are showcased at DAC :

. Availability of an application programming interface (API) that allows programming and integrating Comanche in automated mixed-signal and digital flows using scripting languages like TCL, Perl, Python

. Major performance improvements for netlists with more than multi-million parasitic device.

. User-friendly visualization of most resistive path detection in order to choose source-to-target path analysis

. Integration into the Cadence Virtuoso environment with support the Open Access based versions 6.x

«With these new capabilities, Comanche cuts the simulation cycles even shorter. As an example, Comanche has been used in a production flow in order to determine the effective resistance of a full R network. While the original simulation-based flow took several hours, Comanche generated the same results in minutes», commented Silvant.

Illustration : visualization of most resistive path detection in Comanche available in HI RES-

About Jivaro

edXact's Jivaro technology applies mathematical model order reduction techniques in order to perform netlist

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reduction on netlists generated by parasitics RC-extraction tools. Jivaro is the only tool of the kind that has an absolute error control and thus predictable accuracy. With Jivaro, designers and sign-off engineers are able to carry out accurate post-layout simulations with large amounts of layout parasitics. The simulations are substantially sped up, the memory footprint is reduced. Thanks to interoperability and partner programs with the major EDA vendors, the Jivaro tools are compatible and in production use in all major flows.

About Comanche

Comanche cuts the simulation cycles by carrying out quick layout-parasitics related analyses like the calculating of effective resistance or simplified delay between interconnect ports. Questions like: “what is the exact total coupling between different nets?”, “Is my supply line ok with respect to the ESD design rules?”, “Is the current density on a net critical for the design?”, “Are there gross violations?” and others can quickly, but accurately be answered. Comanche features a GUI and batch version. Comanche has been adopted by customers in production flows in order to carry out sanity checks of the parasitic network.

About edXact

Founded in 2004, edXact SA focuses on electronic design tools aimed at physical verification tasks. edXact’s innovative model order reduction technology helps accelerate backend verifications in complex IC design cycles. edXact is headquartered in Grenoble area, France with sales offices in Japan, Korea, Israel, Taiwan and India.

More information at <http://www.edxact.com>

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