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EdXact sets foot in India

[Anne-Francoise Pele](#)
[EE Times Europe](#)
 06/02/2009 8:00 AM



PARIS — edXact SA, French EDA startup specializing in parametric extraction and physical verification, announced it has selected ICON Design Automation Pvt. Ltd. as its exclusive sales partner in India.

Under the multi-year distribution agreement, ICON Design Automation said it would distribute all of edXact's tools, including Jivaro A, netlist reduction tool for analog and RF designs, Jivaro D, netlist reduction tool for digital and mixed-signal circuits, and Comanche, the company's parasitic rule checking analyzer.

Commenting on edXact's motives to deploy presence in India, Mathias Silvant, president and CEO of edXact, declared: "Our Asian customer base continues to grow, and we won't miss the promising opportunities of India."

He added: "India is a large country with several centers of gravity with respect to the semiconductor industry. ICON is active in all these places with both sales channel and strong team of field application engineers. By partnering with ICON we provide real-time support to our Indian semiconductor customers."

Talking about edXact's customers in India, the company's spokesperson only cited STMicroelectronics Pvt. Ltd. (Delhi, India) to *EE Times Europe*.

Headquartered in Bangalore, India, ICON Design Automation has offices in Hyderabad and Delhi. It is an EDA solutions provider to multinational and Indian design companies in the domains of VLSI, embedded and RF/Microwave.

In October 2008, edXact concluded a similar agreement with New ARTech Technologies Ltd, (Herzlia, Israel) so as to support the company's IDM customers and expand its customer base in Israel. And, in December 2007, the French company signed sales partnerships with EDA Sales, Inc. in San Jose (California) and WIN Technology in Korea.



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The electronics design community is meeting the challenges for greener and more environmentally friendly electronic devices and systems. This was one of the main messages from the SAME Forum held last month in Sophia Antipolis, France.



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Auparavant, pour concevoir un CPU faible consommation, il fallait faire des concessions sur les fonctionnalités, abaisser la fréquence d'horloge, ou encore attendre l'arrivée de nouvelles technologies permettant de réduire la consommation d'énergie nécessaire en mode veille comme en mode actif. Aujourd'hui, ce n'est plus le cas : le monde des processeurs a subi des transformations radicales.



Convergence power multi-corner multi-mode : une nouvelle dimension pour la conception des circuits intégrés

S'il est si délicat de franchir la limite des 65-nm pour produire des circuits intégrés, c'est

What language is most useful for an English-speaking engineer to learn?

- French
 German
 Hindi
 Mandarin
 Russian
 Spanish
 Portuguese
 None because all engineers learn English

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parce qu'il est extrêmement difficile de gérer efficacement la consommation associée.



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