

Bee in the Bonnet, Bug on the Loose



by **Peggy Aycinena**

A summary of recently published EDA product and company news, featured downloads, customer wins, and coming events. Brought to you by EDACafé.

Each period (about twice a month) EDWeekly Review delivers to its readers news concerning the latest developments in the EDA industry, along with a selection of other articles that we feel you might find interesting. If we missed a story that you feel deserved to be included, please contact us! Questions? Feedback? Click [here](#). Thank-you!

There's lots of opportunity for growth and expansion in the EDA industry. Having said that, there's also lots of opportunity for gloom. Cadence's **Chi-Ping Hsu** nixes the gloom opportunity, however, in [a blog posted](#) on the company's site. He says the industry just needs to stay "razor focused" on the problems of the customers and things will work out. I think that's too vague.

Instead, let's consider four specific expansion opportunities. First, there's everything biological – CAD tools for protein design, for neuron/semiconductor interface development, and for labs-on-chip. We've just begun to scratch the surface here.

Second, there's the whole world of nano-everything – in particular, using novel, carbon-based devices to create compute platforms. Too sci-fi for you down-to-earth EDA types? How sci-fi is it that Intel was talking up a 2.3-billion transistor chip at **ISSCC** in San Francisco earlier this month? Have a little imagination.

Third, there's reducing the barrier to access for EDA tools. **Harry Gries** is organizing a roundtable on Wednesday evening, February 25th, at **DVCon** in San Jose to talk about just such stuff – Cloud Computing and SaaS models, "making EDA tools easier to distribute, access, use, scale, and support to make them more affordable for smaller startups and design services companies." Admirable goals. Lots of opportunities.

[**Editor's Note:** Also at DVCon, don't miss the [OSCI events](#) on Tuesday, February 24th, and the [Executive Panel](#) on Wednesday, February 25th.]

Finally, there's the whole multicore/parallel programming problema. And what a problema that is! My conversation below is with Professor Parallel himself, U.C. Berkeley's **Dave Patterson**. We talk about the problems of multicore, the promise of multicore, and the pain of resolving the former to realize the latter.

Meanwhile, at this writing the market is down at a level we ain't seen since October 2002. How gloomy is that? Pretty gloomy – even for those who are "razor-focused" on the future.

And, how is EDA faring in the current economy? Well, SNPS is right on track, selling today at just about what it was selling at in October 2002. MENT is down about 40% from where it sat in October 2002, CDNS is down 60%, and LAVA is down more than 80%.

One question that could be asked given these stats: Why has SNPS maintained its value over the last 6+ years? And, why has it maintained (a semblance of) value over the last brutal 6 months? I'll be talking to Synopsys CEO **Aart de Geus** next month here in **EDA Weekly**, and we'll address that question. We'll also find out if Synopsys is looking at any of the EDA expansion opportunities I've listed above.

It's none of your business ...

If you're a publicly traded EDA company, chances are your recent earnings announcements have not been pretty – unless you're SNPS, of course. If you're privately held, however, the numbers only go

from good to great. Go figure.

- * **Cadence** reported fourth quarter 2008 revenue of \$227 million, compared to revenue of \$458 million reported for the same period in 2007. On a GAAP basis, Cadence recognized a net loss of \$1.64 billion, or \$(6.57) per share on a diluted basis, in the fourth quarter of 2008, compared to net income of \$120 million, or \$0.41 per share on a diluted basis in the same period in 2007. Ouch.
- * **Carbon Design Systems** announced their 2008 calendar year ushered in 27 new customers in "major market segments worldwide" and year-over-year growth of 87%, including Q4 revenue growth of 108% over the same period last year.
- * **ClioSoft, Inc.** announced it ended its 2008 financial year with a 51% growth in bookings over 2007.
- * **CoFluent Design** announced it has doubled its customer base during 2008, "due to the strong technical leadership of CoFluent Studio and a growing market need for virtual system technology."
- * **EVE** announced calendar year 2008 produced year-to-year growth in excess of 30%.
- * **Forte Design Systems** announced "record revenue and bookings" for 2008, including Q4 sales growth of 30%.
- * **Jasper Design** announced a \$7 million Round D influx of cash from **ZenShin Capital**, who are now part of a team that includes **Accel Partners, Cambrian Ventures, Foundation Capital, InnovationsKapital**, and **Northzone Ventures**.
- * **Magma Design** announced a 17% workforce layoff, plus salary cuts and facilities consolidation worldwide. Don't expect champagne and caviar to be served up during the Magma investor call on February 26th.
- * **Mentor Graphics** will also be talking to The Street on their Q4 2008 earning call, in the hour just after Magma's call on February 26th. Given Mentor's predicted earnings for 2009, don't look for any champagne and/or caviar on that call either. It may be interesting to see if the call is executed using VoIP, however. Mentor's received some nice press recently for saving on their phone bills using the latest in Internet technology.
- * **Synopsys** reported results for its first quarter ended January 31, 2009. For the first quarter of fiscal 2009, Synopsys reported revenue of \$339.8 million, a 7.7% increase compared to \$315.5 million for the first quarter of fiscal 2008.

Dave Burrow and Agility ...

I spoke briefly by phone today with **Dave Burrow**, CEO of Agility, which has closed its doors. Burrow confirmed: "Agility sold the assets it bought from Celoxica to Mentor Graphics, and the assets for going from Matlab to C were sold to The MathWorks."

As far as the future of EDA is concerned, he said, "I think the biggest problem for EDA is that it's tough to raise money in this economic climate. [Meanwhile], the issues that Cadence and Magma are having, which are different for each company, make even the normal process of assimilating small companies into larger companies even more difficult than in the past. This process [continues] to take place, but the valuations are weak. Of course, Mentor, Synopsys, MathWorks are strong and will view this time as an opportunity to bring new technology, new products, and new customers into their portfolios."

The real question is, what will happen to the R&D budgets when customers are being more cautious? I don't have a crystal ball, but if you look at data that Wally Rhines has presented in the past, for instance, that electronic design lags the economy by some number of months – if that patterns continues, things will be weak for a while."

Does Burrow think these are good times, nonetheless, for students to consider careers in EDA? He said, "Design problems, in general, are still good opportunities for grad students, but whether they'll

be addressing those problems in EDA companies or in larger electronics companies, I don't know. The geographic distribution of those jobs is also an issue. Will all of the jobs be in Silicon Valley, or even in the U.S.? These are good questions to ask, with no easy answers."

But I do believe technology is still going to be part of the solution – for energy and for making the world more efficient. The mix of the products may change, but we'll see more technology applied to health care, to transportation, to communication – especially outside the U.S."

You just have to remain bullish about technology. The trick is to know where, in which domain, and in which geography the real growth activity will continue. Things always change with time, but the continued role of electronics in the evolution of our society is something you just can't be negative about."

Teddy B.E.A.R.S. picnic ...

U.C. Berkeley's EECS Annual Research Symposium (B.E.A.R.S.) happens every February and is actually just a big advertisement for the Engineering School. It's an opportunity for 10 or 12 faculty members to stand up in front of an audience in the Bechtel Engineering Center on campus and brag on their recent work, their brilliant successes, and various blue-sky ideas that might pan out in the future. The symposium is a not-so-subtle plea for those in the audience – corporate types with access to R&D dollars – to ante up some money to support the Department, the professors, and their students, and not necessarily in that order.

This is the fifth year in a row I've attended B.E.A.R.S. and, once again, I came away with some new ideas and some old prejudices. It turns out, as an aging taxpayer living here in financially troubled California, I've grown a bit tired of the hubris and arrogance of the academics on the stage at my own alma mater.

These guys stand up there (and trust me, there are virtually never any women professors presenting at this dog & pony show) and crow about their projects, their labs, their startups, and the prodigy they've mentored who now drive/own innovation in industry. And, yes those bragging rights are well deserved.

But, as much as these profs want to drive innovation, they also don't want to live without their State-funded safety net. They're happy to step out of academia for a year or two, to act as CTO, or chief scientist, or founder of some zippy start-up, but as soon as the clock strikes midnight on those 2 years – they're right back in the arms of the university, teaching a few classes here and there, and looking forward to retiring on their State-funded pensions and healthcare.

Oh, well. If you're somebody who wasn't smart enough to sign up for lifetime benefits courtesy of the civil service, stop whining. It's too late now. Go out and create something innovative instead. Start a company. Prevail. Win. It's so much more impressive when it's done without a safety net.

Meanwhile, you should really plan to attend B.E.A.R.S. every year going forward. Lots of cool engineering, free breakfast and free lunch. Doesn't get much better than that. Just ask **Ted Vucurevich**. Even he was at B.E.A.R.S. on the Cal campus on February 12th. Nice to see you, Ted!

Bug-bots ...

When I was little, I knew kids who liked to fry bugs under a magnifying glass. I was reminded of same when I saw the B.E.A.R.S. presentation by **Prof. Kristofer Pister** with footage of a fly-by-wire moth that his students rigged up using a chip-in-bug-brain device that allowed them to tell the moth to turn right or left in flight.

Ironically, two days before, researchers from the **University of Arizona** demo'd the exact same type of work to an SRO crowd at **ISSCC** in San Francisco. The UofA configuration also consisted of an invasive device, but theirs was attached via harness to the belly of a big ol' beetle, allowing them also to make their bug-bot turn right or left in flight. Meanwhile, **IEEE Spectrum** is currently bragging on similar work from DARPA.

Query: If there are Three Laws of Robotics, are there also Three Laws of Bug-botics?

Lest Stanford feel slighted ...

For those among us who receive the Annual Report for **Stanford's School of Engineering**, I would recommend turning to page 21. There, traveling incognito in a photo-sans-caption, is Stanford's Favorite [EDA] Son, **Dr. Walden Rhines**.

Probably just capricious that listed in the column to the left of the photo, under the category of "Other" Endowed Faculty Funds, you'll find a mention of the **Cadence Design Systems Directorship in the Computer Systems Laboratory**. And here I thought Cadence was Blue & Gold through and through. (Dr. S-V, what's that all about?)

Meanwhile, it's important to note the **Dr. Rhines** was named a **Fellow of the International Engineering Consortium** (IEC) at **DesignCon** earlier this month. Following his award, Rhines gave a [rousing keynote](#), now available online and worth the half-hour spent viewing. Rhines reviews the history of EDA, and waxes poetic about reasons for hope and enthusiasm within the industry.

Professor Parallel ...

Dr. Dave Patterson has been teaching at U.C. Berkeley for over 30 years, after doing his undergrad and graduate work at UCLA. Patterson's technical accomplishments are immense. He coined the term RISC, authored 5 books (2 of them with his fellow RISC innovator, Stanford President **John Hennessy**), was President of the ACM from 2004 to 2006, is an ACM, IEEE and AAAS Fellow, a member of both the National Academy of Engineering and Science, and a walking encyclopedia w.r.t. RAID, NOW, RAD, and RAMP. Patterson also raises money for MS research by riding his bike hither and yon.

Most importantly, he's a certified expert on everything parallel on all things multicore. On February 11th, Dr. Patterson and I spoke for an hour by phone. It was a great interview. I asked questions. He talked. I typed.

Q: What is multicore?

Dave Patterson: Anything with multiple processors on a single chip.

Q: What is multithread?

Dave Patterson: That's more complicated. It's about trying to get more performance out of a single core by running multiple threads on a single core.

Q: What's parallel processing?

Dave Patterson: In general, that means running multiple programs in parallel on multiple cores. From a programmer's perspective, you would write the program as if you thought it was running on multiple cores. The hardware is just going to run those threads on the processors assigned, but the hardware's not smart enough to decide which thread should run on which processor. Typically, it's best to think about these questions on two different axes. One is multicore and one is multithread.

Q: What's the state of the art today?

Dave Patterson: Today, we have desktop microprocessors that have 2-to-8 cores on the chip. It's speculated that going into the future, the number will double every five years, going to 16, then 32, and so on. In terms of multithreading, today you have multicore chips with 1, or 2, or 4, or 8 threads running. To understand the full capacity of a system, you multiply the two numbers together. If there are 8 cores with 8 threads, it would appear as if there were 64 threads running in parallel.

Q: Why is it so important to do this?

Dave Patterson: It makes the hardware more effective, which means you get more value out of the hardware. From a programmer's point of view, however, I've got to find a way to make programs [in such a way as to capitalize on the available hardware].

Q: I went to a tutorial at ESC in Boston in 2007 where the instructor said "allegedly-multicore" systems are being shipped where all but one core is effectively turned off. Multicore is really just a lot of marketing hype. So, if you buy a laptop with an 8-core chip, the programs are only using a single core out of the 8.

Dave Patterson: That was a clever thing for the instructor to say, but it's not true. In any laptop, or desktop, or server, there's always an OS running plus other applications, so you can easily keep a couple of cores busy. If your system is multicore, for instance, you can actually set up a performance measurement, so you can see at any time how busy each cores is.

Q: So alternatively, why not just ship systems with one big, honking single-core processor, and let clever software do the gatekeeping and load balancing between applications running on that single core?

Dave Patterson: That's actually the attractiveness of parallel processors – you don't have to design huge new hardware. You can just use multicores.

What actually happened until just a few years ago is, they built bigger and bigger microprocessors so programmers didn't have to work out the problems of parallel programming. But then, the processor used more and more power, and at 100 watts per chip, that was the most it could handle without exotic packaging.

By 2004 or 2005, we ran out of what we could do with your 'honking' single-core microprocessor and the only path forward was to replace it with 2, more power efficient cores. But, if we could still do it with a single processor, it's true – we wouldn't have to [bother with the problems] or multicore. If you could buy a 15 GHz processor, [we'd be set]. If we could have 500 Watt chips, we could have 15 GHz, but the only possible way to get there is through multicore.

Now the situation is more than just choosing between the lesser of two evils, single core or multicore. There's actually only one fork left in the road. [Meanwhile], people have worked for 15 years to build hardware that preserves the single processor illusion for programmers. It's something that many smart people have worked on in the past, and it's where we have failed. But the future of the industry [rests in our ability to get] more performance in this pretty well trodden area. It's remarkable that it's taken so long.

Q: So, what is the secret sauce to parallelizing complex algorithms for coding?

Dave Patterson: You mean, how to just cut the Gordian Knot? Well, we're not there yet. Or another way of describing it – do you know football? What we need is the Hail Mary pass.

But even then, it's a lot easier to throw the Hail Mary pass than it is to catch it. A bunch of us – not just at Berkeley, but in lots of places – are trying to figure out a way we can catch it. We're trying to demonstrate ways to help more people build parallel programs, but it's really hard to do. We're all researchers involved in work that will make these ideas more operable.

Q: I heard Kurt Keutzer's talk at DAC last year about creating buckets for different types of programs, an attempt to classify programs into buckets that lend themselves more or less easily to parallel programming – if I understood the gist of his presentation.

Dave Patterson: Kurt's office is right across the hall from mine here in Soda Hal! Yes, Kurt's right. This is the El Dorado, this idea of identifying design patterns in software architecture. If we think more carefully about the architecture of the software while we're building the software, many of those applications would lend themselves to parallel execution.

[Unfortunately], often people have ignored software engineering, so we're betting that by carefully architecting your software into one of these well-known patterns, it will be easier to parallel program.

Q: Are you telling me that we're only now starting to teach tidy programming practices?

Dave Patterson: No, what I'm saying is the difficulty in teaching is that you've got just about one semester to teach a student to program. During that semester, the students write maybe 1000 lines of code, maybe 10,000, with which to learn the programming principles of software engineering. It's very difficult to teach these things, to teach concepts that are important industrial concerns when they don't necessarily work in the classroom.

[Also], it's hard to quantize [the value] of good programming principles. People have been talking about software architecture for a long time, but still it's hard to tell how seriously people take it.

Kurt Keutzer always knew, particularly when he was CTO at Synopsys, that software architecture is overwhelmingly important. It's his insight that has led us to examine the hypotheses that we should be sensitive to design patterns – and now we're demonstrating it. People are starting to get impressive results, and we won't need to have the Single Golden Truth about parallel programming to solve the problem.

That Hail Mary pass? It's in the air, and researchers everywhere have a sense of urgency that comes from wanting to beat their competition in catching the pass. It's really an unusual circumstance – lots of people in industry needing the answer and waiting for us for us to find it.

Q: If it's so important to industry, why doesn't industry solve it themselves?

Dave Patterson: They are! They're funding work at Illinois, at Stanford, at Berkeley, and other places. Not all of the best minds are at one company or at one university.

Q: And whoever gets the answer will own the patent?

Dave Patterson: I'm actually a patent skeptic – I've never filed a patent. It's too easy to get around patents. The more important thing is to demonstrate an idea, and then to convince people that you've got the answer.

I like the Berkeley Software Distribution Model, the BSDM. We're happy to have our software in open source. In areas like pharmacology, where it takes 10 years to do research, it's a different story. But, that's not the case in IT. Our philosophy is to work openly with industry.

Q: So, who's in this race with you to catch the Hail Mary pass?

Dave Patterson: University of Illinois. Also, Microsoft and Intel, Stanford, AMD, Nvidia, and others. Here at Berkeley we've assembled a really great team and we're making really exciting progress right now. Of course, everyone I mentioned has got a big team, as well, and good people working to solve this for the country and the world. It's also really important that we're all taking different approaches to finding the solution.

Q: Why not have a NASA/NACA-type program funded by the government? The American aviation industry was built on basic research, wind tunnels, etc, funded by the U.S. Government in the first half of the 20th century. If the parallel programming problem is so important, why not do it the NASA/NACA way?

Dave Patterson: Actually, when I was President of the ACM, I wrote several editorials on this topic. The Administration was cutting back on funding for academics. I wrote that some years down the road we'd need solutions, but since DARPA wasn't funding the work, we wouldn't have them when we needed them.

Why wasn't DARPA funding brilliant students at great universities? They were funding industry instead – shorter-term stuff – giving hundreds of millions of dollars to companies like Cray and Sun and IBM. Actually, the person in charge of DARPA [responsible for those decisions]? His term just ended yesterday!

I'm pretty much on the record saying that what he did was terrible and American IT research has

suffered as a result. If he had not changed the model 8 years ago, made decisions to the detriment of our country, it would be a very different world today.

[Meanwhile], other countries like China and India have stepped up their investment in IT. Parallel computing is something they'll try to do research on. Industry everywhere wants somebody to catch [that Hail Mary pass]. If somebody catches the pass in China or Korea or India – the first people to make the catch will have a head start.

Q: How will you know when you see the answer? Maybe you'll see the solution published one day in the Communications of the ACM?

Dave Patterson: If you [listen to some people] out there, it's apparently easy to write programs that can run on hundreds of cores. The programs are correct, they don't waste energy, and as the number of cores increases over time, the programs run even faster. But it's not that easy.

This idea that somebody sitting in their garage will invent this – that some teenager playing video games will suddenly discover parallel computing – it's not going to happen. We need [sufficient] amounts of money to fund grad students, enough for them to live on. That's not much by industry standards, but it's huge by academic standards.

Also, there may be some startups claiming to have solved the problem, but I don't know of any research papers where people are claiming to have done it. However, if somebody does have the answer out there, and it works, they'll make a lot of money, or a lot of fame.

Q: Which is more important? The money or the fame?

Dave Patterson: I'd pick the fame. I've seen a lot of people with money, but it doesn't solve as many problems as you'd think.

Q: So, when will parallel programming be solved? What's a realistic timeframe?

Dave Patterson: I think we'll make progress soon. After all, we've only been doing this for a year – this search for patterns. So far, we've made some pretty impressive progress on 4 programs that are important, so I think we'll make significant progress over the next 10 years. But given how hard it still is today, if you were to tell people that we're going to solve this problem in 10 years, they would either be impressed or shocked.

If you look at President Kennedy announcing in 1961 that we would land a man on the moon within 10 years, it was the same as with this parallel programming problem. Nobody believed it!

[Editor's Note: To hear Dave Patterson's talk about the work of the Parallel Computing Lab at U.C. Berkeley, click here; [http://www.eecs.berkeley.edu/BEARS/.](http://www.eecs.berkeley.edu/BEARS/)]

Connect the dots ...

So let's be patently ridiculous and say there really is some good news coming out of EDA. Read on at your own peril, however, because you might inadvertently feel optimistic about the future.

* **Apache Design Solutions** announced expanded business relationship and technical collaboration with **STMicroelectronics**. Previous collaborative efforts produced "power and noise solutions for SoC power signoff, advanced low power design validation, custom IP analysis and modeling, and early-design power/ground grid prototyping." ST R&D VP **Philippe Magarshack** is quoted: "By collaborating with Apache, we expect to address early on the global power and noise issues brought by the 45/40nm and 32/28nm technology nodes."

* **Atrenta** announced that **Atheros Communications** has adopted Atrenta's SpyGlass- CDC product. Per the Press Release: "Atheros will broadly deploy the tool to help reduce design risks associated with semiconductor IP integration."

* **Berkeley Design Automation** (BDA) announced AFS Nano, "a version of Analog FastSPICE with a

5K-element capacity limit for only \$1,900 ... delivers true SPICE accuracy 5x-10x faster than traditional SPICE for complex blocks ... [estimates say] 50% of the SPICE simulators are used for block-level runs, which will comfortably fit within AFS Nano."

* **Cadence** *grand-opened* its new San Jose building on Monday, February 9th. No offence taken that I wasn't invited to the opening, but heard about it from folks who did: Fancy new digs, with guesstimates from industry observers that a consolidation of headcount from others buildings at the San Jose campus is next. Those same observers opined that by 2010 Cadence will be a "nice \$250 million boutique EDA company." Only time will tell.

Also, no offence taken that **John Blyler** actually snagged an interview with **Lip-Bu Tan**. His notes from the interview are brief, but informative. The fact that Tan is now on the EDAC Board as reported by **Gabe Moretti**, means at least we'll see Tan at the 2010 CEO Forecast panel.

I look forward to distributing the wine once again at that event for anyone sitting in the back third of the room. In the good old days, it fell to the then-management gang from Cadence to pass the wine around at the back of the room at [EDAC events](#). Happily, I suspect the new management team at Cadence will not be exhibiting that particular behavior anytime soon.

* **Calypto Design Systems** announced a collaboration with **ARC International** to reduce power in ARC's low-power video subsystem IP using Calypto's PowerPro CG.

* **Carbon Design Systems** announced an expanded model portfolio working with **ARM** to create IP, and partnering with Tensilica to distribute that company's processor models.

* **CCG Facilities Integration** announced it used FloVENT software from **Mentor Graphics'** Mechanical Analysis Division (formerly Flomerics) to "optimize the design of Dupont Fabros Technology's (DFT's) ACC4 data center in Ashburn, Virginia. The challenge was to design a system to cool the extremely powerful and hot computing and communications equipment occupying the data center while maintaining a Tier 4 level of functionality. "FloVENT provided the ideal tool for optimizing the performance of ACC4 because of its ability to accurately model the room, the IT equipment and complete cooling system," Margaret Sam Sheehan, Director of Mechanical Engineering for CCG, said via the Press Release.

* **CoWare** and **Rambus** announced a collaboration on "a comprehensive ESL design environment with CoWare Platform Architect for Rambus' XDR memory architecture. CoWare will distribute a SystemC model ... to match configurations of Rambus' XDR memory subsystems."

* **DAC** announced that nominations for the **Marie R. Pistilli Women in EDA Achievement Award** will be accepted until Friday, April 10. The 46th DAC will be held July 26th-31st at the Moscone Center in San Francisco.

* **DATE 09** announced it will co-locate with the **ARTEMISIA Association** conference in Nice, France, during the week of April 20th. Per the Press Release: "[This move] will increase attendance to over 5,000 researchers, engineers, executives and policy makers from industry, academia and public authorities. The ARTEMISIA Association was founded to strengthen Europe's advanced research and technology position in embedded intelligence and systems."

* **EDXACT** announced it is "a major contributor in the joint development project, **CILOE**, led by **Minalogic**, to help small-to-medium size enterprises develop massively parallel and optimized versions of their software on threaded processors and computing farms. **CILOE (High Performance Computation for EDA and embedded applications)** aims at developing a complete computational infrastructure, including methodologies, software, and security mechanisms in order to facilitate small and mid-sized enterprises access to this kind of technology."

* **EVE** announced synthesis capabilities, zFAST (ZeBu Fast SynThesis), which the company says will handle large designs with "a bottom-up and top-down approach targeting its ZeBu (for Zero Bugs) emulation systems." EVE-USA GM **Lauro Rizzatti** is quoted: "New designs reach tens of millions of ASIC-equivalent gates, with processor and graphics designs moving well into several hundreds of millions gates. Mapping such large designs into a large array of FPGAs break many commercial FPGA synthesis tools. zFAST was developed for these types of designs."

- * **Forte Design Systems** announced **Dave Tarpley** has been named Vice President of Japan, reporting to Marketing & Sales VP **Brett Cline**. Per the Press Release: "Tarpley brings more than 35 years of management and sales experience to the position, holding senior executive and sales management positions for various companies within the electronics and EDA industry."
 - * **GateRocket** announced its RocketDrive for **Altera's** Stratix IV FPGAs. Per the Press Release: "The RocketDrive cuts verification and in-system debug time for advanced single or multi-FPGA based projects while adding significant value through seamless integration with a design team's existing verification environment, with no changes to the flow or verification methodology."
 - * **ImpulseC** announced a new FPGA development kit for high-throughput video processing. Per the Press Release: "Even if you are primarily software focused, our tools are for you – over half of our customers have never designed hardware previously. Using our design environment you can create complex systems much more easily than hand coding in HDL."
 - * **Jasper Design** announced **Holly Stump** has been named Vice President of Marketing. Per the Press Release: "Stump's experience includes high-tech B2B marketing, business development, channel management, and international sales experience in the EDA, semiconductor, and electronics industries."
 - * **Jasper** also announced its **Design Activation Services** "to help both design houses and commercial IP vendors reap the benefits of design and IP reuse, amortizing research and development costs over multiple IC design projects. Jasper's new service ... consists of specialized consulting to deliver an Activated Design – an executable design database – for a particular design block, several blocks, or an entire library."
 - * **Javelin Design Automation** announced a solution, developed in conjunction with **IMEC** and **Qualcomm**, for "rapid design exploration and optimization of 3D stacked ICs (3D SIC). Per the Press Release: "3D PathFinding extends the Javelin PathFinding methodology and j360 Silicon PathFinder platform to support virtual chip design for co-optimization of system design and 3D interconnect-packaging technologies. With turnaround times of a few hours or days, designers can evaluate and optimize their system and micro-architecture to best exploit 3D technology options; and silicon process engineers can fine-tune their technology to the system architecture specs."
 - * **Magma Design** announced that **LogicVision** has licensed Magma's ATPG technology. Per the Press Release: "The agreement enables LogicVision to accelerate the expansion of its product portfolio and provide customers with comprehensive DFT capabilities. An additional agreement allows Magma to distribute LogicVision products to customers."
- "Magma will continue its focus on core products in implementation, physical verification and circuit simulation while LogicVision provides DFT technology expertise including support for advanced ATPG technology," says the Press Release quoting **Kevin Moynihan**, GM of Magma's Design Implementation Business Unit.
- * **Materialise** announced a collaborating with **ANSYS** to provide product interoperability. Per the Press Release: "The latest Mimics 12.1 version enables users to export to the ANSYS Workbench format, [which] will facilitate the workflow for the fast-growing Mimics user community, leading to successful bioengineering worldwide."
 - * **Mentor Graphics** announced it has appointed **Robert Hum** as vice president and general manager of the Deep Submicron Division, **Glenn Perry** as general manager of the Embedded Systems Division, and **Guy Moshe** as general manager of the Design Creation business unit in the Design Creation Synthesis Division.
 - * **OneSpin Solutions** announced "mainstreamed" formal assertion-based verification (ABV) for SoC, ASIC and FPGA designs through "a structured, step-by-step approach to its use and adoption ... [using] five interoperable products in a new, integrated 360 MV product family." OneSpin also announced "a new proof-based debugger for complex SystemVerilog Assertions (SVAs) [which] automatically locates the root-cause that makes an assertion fail."

* **Open Virtual Platforms** (OVP) has released new native SystemC transaction level modeling (TLM)-2.0 technology to use with OVP CPU models that run to the speed of one billion instructions per second (1,000 MIPS). These models were developed by **Imperas** and are free to download at www.OVPworld.org site. "These are the fastest CPU models available and we are now making them available for free to the SystemC community to work with native TLM-2.0," Imperas CEO **Simon Davidmann** announced via the press release.

* **Real Intent** celebrated its 10th year in business and is offering existing and new customers two copies of its software for the price of one copy.

* **Sigrity** announced its Channel Designer analysis and simulation tool for designs with high-speed serial links such as PCI Express. The new product lets designers implement the communications backbone for GHz-speed design, "addressing accuracy challenges ranging from feasibility studies to design implementation."

* **SpringSoft** announced that Seiko Epson Corp. extended the terms of its volume purchase agreement for the SpringSoft Verdi Automated Debug System.

* **Synopsys** announced two improvements to its PrimeTime STA suite, which the company says includes "a flexible multicore processing technology that makes more effective use of both single-core and multicore CPUs across today's compute server farms."

* **Tensilica** announced its Bluetooth sub-band codec (SBC) decoder and encoder for its HiFi 2 Audio DSP.

* **X-FAB** has announced 5 new options in its 60nm BiCMOS platform especially for optoelectronics applications, including a light shield module that protects light-sensitive areas, and a light-sensitive Blue pin module.

You can find the full EDACafe event calendar [here](#).

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-- Peggy Aycinena, EDACafe.com Contributing Editor.
