



## PRESS RELEASE

### **EDXACT delivers enhanced versions of Jivaro and Comanche at DAC**

*All tools are connected on a new common proprietary parasitic database*

*Jivaro 4.2 and Comanche 2.0 will be demonstrated at booth 455  
Design Automation Conference in Anaheim, California, June 9-12.*

**GRENOBLE, France, May 28, 2008.** Backend verification specialist edXact SA today announced that Jivaro, its netlist reduction tool and Comanche, its IC interconnections analysis tool, are now based on a common proprietary parasitic database. This further boosts each tool's performance and enables a seamless combination to explore, analyze or reduce huge RLCK parasitic networks. edXact (Voiron, France) is a provider of innovative tools aiming at accelerating detailed simulations within existing semiconductor design flows, while maintaining accuracy. Version 4.2 of Jivaro and version 2.0 of Comanche will be demonstrated at the Design Automation Conference in Anaheim, California, June 9-12.

"During the past year, edXact has been improving its products offering by building a common platform, called TOTEM, which combines a proprietary mathematical data base and a large set of innovative, efficient and accurate reduction algorithms," stated Mathias Silvant, edXact President. "The simplified database greatly enhances model order reduction performance and also facilitates the implementation of future new features, like incremental netlist reduction."

#### **Explore, analyze and reduce**

Three products are now based on the new platform and database: the two flavors of edXact's flagship netlist reduction tool - Jivaro HD for mixed-signal and digital design, and Jivaro A for analog and RF design - and Comanche, their companion analysis tool. Comanche helps detecting gross errors in the design's interconnections, which are extracted as huge parasitic networks. "Comanche can be used before the netlist reduction tool. It can be used to judge if a full-flavoured simulation lasting several hours is useful by eliminating a number of recurring design problems", comments Silvant.

#### **New products features**

The comprehensive software suite for IC nanometer design helps backend physical verification teams to reduce time to market by enabling and speeding up post layout simulation of huge RLCK extracted circuits, while keeping a very high accuracy.

*Jivaro 4.2: improved memory usage and simpler control*

JivaroHD is a parasitic reduction software for digital designs ; it deals with DSPF, SPEF and now Mentor's CalibreView format files. Compared to previous versions, JivaroHD 4.2 brings the following additional features :

- The ability to handle controlled sources
- The ability to change net's topologies before reduction.
- Improved and simpler control of the reduction process.
- An API for programmable integration into automated verification flows.

Performance, memory usage and reduction rate have also been improved in order to handle very large nets (like power supply).

*Jivaro A 4.2: new reduction algorithms*

Jivaro A is a parasitic reduction tool dealing with Spice, HSpice, Eldo and Spectre format files. Compared to previous versions, Jivaro A 4.2:

- Can handle interconnect parasitic networks with a large number of ports.
- Can now also reduce controlled sources.
- Handles directly parasitic extracted views of the Cadence CDBA database.

The SALSA GUI option, giving access into Jivaro A and Jivaro HD from the Cadence environment, has been improved to allow pre- and post-processing tasks.

*Comanche 2.0: additional parameter calculations and a new GUI*

Comanche is an exploration and analysis tool dealing with DSPF and SPEF format files and calculating pin to pin parasitic impedance values. Gross impedance errors in turn pinpoint errors such as wrong vias that can easily be corrected before launching timely simulations. Compared to Comanche 1.0 which mainly calculated resistances, Comanche 2.0 also calculates capacitances, Elmore delays, and S/Y/Z parameters which can be output in Touchstone format. A GUI has also been added to set the options and inspect the results.

**About edXact**

Founded in 2004, edXact SA focuses on electronic design tools aimed at physical verification tasks. edXact's innovative model order reduction technology helps accelerate extensive backend verifications in complex IC design cycles. edXact is partnering with all major EDA vendors' interoperability programs. The company's headquarters are based in Grenoble area, France.

For additional information, please visit our web site: <http://www.edxact.com>

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