



Wednesday, January, 2nd 2008

News Analysis

Ten 2008 trends in system and chip design

By Richard Goering

01/02/08

Prediction is always a risky business, but in the world of chip and system design, there are some new methodologies, tools, and challenges that are clearly going to impact design and verification. This article examines those developments in order to identify ten top trends for 2008.

What's driving all of these trends is design complexity. Consumer electronics, for example, is bringing about a new generation of mobile, multi-media devices that must support multiple application and interface standards, low power, and fast time to market. And in every application area, the pressure is on for solutions that are higher in performance, lower in cost, and no hungrier for power consumption than what came before. These demands are behind the move to 65 and 45 nm ICs, the emergence of complex architectures, and the explosion of embedded software content.

The 10 trends identified here are the following:

1. Functional verification gains intelligence
2. New approaches boost analog/mixed-signal design and verification
3. Virtual platforms speed software development
4. Advanced power techniques raise verification challenges
5. EDA applications move to parallel computing
6. As 45 nm hits production, DFM challenges rise
7. IP trends: configurable processors, mixed-signal cores
8. Memory importance and options increase
9. FPGA design is more like ASIC design
10. Packages and boards come into the picture

1. Functional verification gains intelligence

Long regarded as the biggest single bottleneck in IC design, functional verification received increasing attention in 2007, and will become more intelligent and automated in 2008. Some years ago Gary Smith, chief analyst at [Gary Smith EDA](#), put forth the vision of an "intelligent test bench" that would evaluate a design and apply the correct verification engines to various blocks. The full scope of that dream has remained elusive, but developments in 2007 suggest that we're at least heading in the direction of smarter verification.

There was some interesting startup activity in 2007. [Certess](#), for example, introduced "functional qualification," a new approach to verification coverage that profiles tests, injects faults, and then determines if the existing verification testbench would have detected them. [Breker Verification Systems](#) introduced a graph-based functional "test synthesis" tool that provides automatic test vector generation. And [Nusym Technology](#), which has yet to formally announce a product, is working on technology that automates both coverage estimation and test generation. Another company to watch in 2008 is [Mentor Graphics Corp.](#), which quietly [bought startup Lighthouse Design Automation](#) and acquired technology that promises high coverage through intelligent testbench generation.

"2008 will herald a more holistic, intelligent verification approach, with EDA tools using coverage data to accelerate the entire verification process in an automated manner," said Venk Shukla, president and CEO of Nusym. "By intelligently using key coverage metrics to select and generate the vital test sets from the overly verbose pseudo-random vector sets, potential quality issues may be directly targeted with a reduced [complexity], high-impact testbench."

Functional qualification metrics will make third-party silicon intellectual property (IP) more trustworthy, said Mark Hampton, founder and CEO of Certess. "Functional qualification is a simple concept of measuring the ability of functional verification to find design bugs," he said.

There's a constant and growing demand for "helper" applications that make the verification flow more rigorous and productive, said Scott Sandler, CEO of [Novas Software](#). While automating debugging is one example, another is "the new class of tools in the verification closure space." These new tools, he said, include formal analysis, coverage estimation, and power-aware verification.

Formal property verification will see widespread deployment in 2008, according to Craig Cochran, vice president of marketing at [Jasper Design Automation](#). He said that formal verification is finding two new applications. One is "RTL exploration" that allows designers to quickly validate their ideas, and another is post-silicon debugging, in which formal tools can help identify the root cause of a bug and verify that it's fixed correctly.

Meanwhile, standards efforts may help make verification environments more open and interoperable this year. In 2007, [Cadence Design Systems](#) and Mentor Graphics developed the Open Verification Methodology ([OVM](#)), an open-source SystemVerilog class library and methodology that defines a framework for reusable verification IP and tests. "One clear dominant trend in verification is the move away from proprietary, tool-locked verification methodologies toward an open methodology," said Jim Miller, executive vice-president of the product and technologies organization at Cadence.

Another emerging standards effort is the Accellera Unified Coverage Interoperability Standard ([UCIS](#)), which is developing an API that can [unify coverage data](#) from different types of tools, including simulation and formal verification.

2. New approaches boost analog/mixed-signal design and verification

Analog/mixed-signal design and verification will move forward in 2008 in at least two significant ways. First, new methodologies and tools will bring more rigor, precision and speed to analog verification. Secondly, the move towards interoperable parameterized cells (p-cells) and process design kits (PDKs) will pave the way for more startup activity and more tool choice for users, challenging Cadence Design Systems' traditional market dominance in analog IC design.

In a recent [Expert's Corner interview](#) on SCDsource.com, Henry Chang, co-founder of [Designer's Guide Consulting](#), outlined an emerging analog verification methodology that uses behavioral modeling and regression testing. Driving the need for this methodology, he said, is the increasing architectural complexity needed to support multiple standards, demanding specifications, and low power. "Applying more rigorous, systematic, and automated approaches in analog circuit verification will become more critical in 2008," Chang said. "The concept of having a separate person or team responsible for analog circuit verification will gain more traction."

Tom Borgstrom, director of solutions marketing at [Synopsys](#), also foresees new analog/mixed-signal (AMS) verification approaches. "Increasing mixed-signal content will drive the emergence of new AMS verification methodologies that leverage successful approaches used in digital functional verification, while providing hierarchical techniques that use functional blocks directly in their native modeling languages," he said.

"In 2008, the EDA industry will need to bridge the gap between digital and analog design, and bring digital-type automation to the analog designer," said Ashutosh Mauskar, vice president for product and business development at [Magma Design Automation's](#) custom design business unit.

Circuit verification of analog and mixed-signal blocks "is getting close to impossible," said Mathias Silvant, CEO of physical verification provider [Edxact S.A.](#) He said that "all means" will be employed this year to solve that problem, including model order reduction, enhanced fast Spice simulation, and behavioral modeling. Paul Estrada, chief operating officer of circuit analysis provider [Berkeley Design Automation](#), said that analog and RF designs need to be verified at a higher level of hierarchy. "There will be a shift to analog/RF verification tools that can deliver complex block and full circuit verification with full Spice accuracy," he said.

Analog and transistor-level verification has become a ripe area for startups. In 2007, [Solido Design Automation](#) introduced transistor-level statistical design technology that promises new functionality well beyond conventional Monte Carlo simulation. [Xoomsys](#) is developing a parallel Spice capability. [Nascentric](#) rolled out a multi-threaded fast Spice simulator last summer.

Meanwhile, one of the most significant developments in analog IC layout is the development of interoperable p-cells, which are a critical part of every foundry PDK. Until very recently, nearly all p-cell libraries were written in Cadence's proprietary Skill language, and were generally not portable to other vendors' tools. Startup [Ciranova](#) pioneered interoperable p-cells for the OpenAccess database in 2006, and last year, five vendors collaborated to develop an open-source, interoperable p-cell library ([IPL](#)) generated using technology from Ciranova.

"2008 will see the first practical implementation of interoperable p-cell libraries built on the Open Access database," said Rich Morse, director of marketing at IPL co-founder [Silicon Canvas](#). "For the first time there will be an open environment for custom integrated circuit design, beginning a sea change in the last single-vendor EDA monopoly." Eric Filseth, CEO of Ciranova, said that the first interoperable PDKs from foundries will appear in 2008. Until now, he noted, foundry design kits have used proprietary formats and worked with tools from a single vendor.

3. Virtual platforms speed software development

Electronic System Level (ESL) providers have been trying to raise the IC design abstraction level for years, with limited success. But one ESL application that has been receiving increasing attention, and that promises to become even more prominent in 2008, is the use of virtual platforms (also known as "software virtual prototypes" or "virtual prototypes" or "virtual system prototypes.") Virtual platforms provide a system-level model that's fast enough for software development and accurate enough for architectural exploration and optimization. As noted in a recent [SCDsource feature story](#), virtual platforms are finding satisfied users today at system and system-on-chip (SoC) design companies such as AMCC, Freescale, General Dynamics, Infineon, Sarnoff, STMicroelectronics, and Wind River Systems.

"2008 will be the year of the virtual prototype," said John Sanguinetti, CTO of [Forte Design Systems](#). "In 2007, most large design projects attempted to use virtual prototypes in one form or another. In 2008, designers will be trying to improve the prototyping process to get more acceptable speed, accuracy, and overall usability from their prototypes." A byproduct, he said, will be demand for higher level silicon IP.

"The growing use of virtual platforms for pre-silicon software development is being fueled in part by the establishment and adoption of open standards for constructing the transaction-level models that serve as the building blocks for these platforms," said Matt Gutierrez, director of marketing for professional services and system-level solutions at Synopsys. He noted that the Open SystemC Initiative ([OSCI](#)) Transaction Level Modeling (TLM) 2.0 draft 2 should facilitate TLM interoperability across companies and design tools. OSCI recently [released that draft for review](#). The lack of TLM interoperability has been [cited as a major obstacle](#) to the acceptance of virtual platforms.

While ARM, Carbon, CoWare, Synopsys, Vast Systems, and Virtutech offer virtual platform tools today, [Imperas](#) plans to offer virtual prototyping in early 2008 for multicore ICs. Imperas will provide simulation, debugging, and a model library. It's a [change of focus](#) for the much-watched startup, whose original goal was to provide a high-level software programming environment for multicore ICs.

"2008 will be the year of the integrated compiler, profiler, and virtual platform," said Mark Snook, director of marketing for [ARM](#). Combine a virtual platform with a compiler that can optimize code generation, and a profiler that's aware of operating threads and resources, "and you have a killer suite of tools," he said.

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