

## **EDXACT delivers version 4.0 of Jivaro technology at DAC**

### ***Important increase in capacity, GUI in Cadence Analog Environment***

**GRENOBLE, France, May 28, 2007.** EDXACT SA today announces that its JIVARO netlist reduction technology and its COMANCHE interconnection analysis tool both are released in new versions. In addition to numerous additional features, capacity increase, support of inductance and mutual inductance in large files in custom flows and a Graphical User Interface into the Cadence Analog Environment are the most predominant innovations.

Version 4.0 of JIVARO HD (high density) and version 1.1 of COMANCHE will be demonstrated at the Design Automation Conference in San Diego, California, June 4-8, 2007.

Provider of a parasitic data management & analysis platform, EDXACT (Grenoble, France) has enhanced its proprietary technology, allowing for a substantial increase in capacity for the products that are built upon it, including JIVARO and COMANCHE. These tools help IC designers to optimise post-layout simulations, to maintain verification accuracy and to meet time-to-market goals.

#### **JIVARO HD: high volume, power nets and ease of use**

The JIVARO family of tools performs the reduction of parasitic files obtained from layout extraction tools, before feeding them to simulation tools, achieving dramatic speed improvements. The 4.0 Release (dubbed HD for high density), increasing its capacity to several tens of Gigabytes for nets with RLCK elements is a powerful tool when used with designs targeting 90 nm, 65 nm geometries and below. An accrued need for more detailed parasitics in design and postlayout verification comes along with those modern technologies.

JIVARO HD brings another capacity enhancement regarding the length of the nets that can be handled and the number of ports to one and the same net, as well as the number of parasitic elements accepted on the same net, which is dramatically increased. As a result, the tool is now able to perform outstanding remodelling of power nets.

EDXACT also extended the tool's unique capability to select parts of the netlist and to assign accuracy levels in order to optimize the trade-offs between accuracy and simulation speedup. "Model order reduction replaces the parasitic model by an equivalent model of smaller order", explains Corine Lamagdeleine, EDXACT's Product Marketing Manager. "Designers now can select accuracy levels based on the delay or frequency on a net".

#### **S-parameter data now issued by COMANCHE 1.1**

Along with an important increase in capacity, COMANCHE 1.1, the latest upgrade of EDXACT's analysis tool to be showcased at DAC, is now able to compute S-parameter data between ports in high frequency circuits. Outputs are in Touchstone compatible format, so that the designer can enhance its HF simulations with detailed S-parameters computed by COMANCHE.

By taking parasitic netlists and computing global values of interconnection resistance, impedance and delay, as well as S, Y and Z parameters for sets of ports, COMANCHE is a powerful analysis tool helping to rapidly pinpoint gross violations before simulation.

**About EDXACT**

Founded in 2004, EDXACT SA (Electronic Design: eXtraction, Analysis and Control Tools) focuses on electronic design tools aimed at physical verification tasks. EDXACT's innovative model order reduction technology helps accelerate extensive simulations needed for backend verifications in complex mixed-signal IC design cycles. EDXACT's headquarters are based in Grenoble area, France. For additional information please visit EdXact online at [www.edxact.com](http://www.edxact.com) or send your questions to [info@edxact.com](mailto:info@edxact.com).

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