



## PRESS RELEASE

### A major Japanese IC supplier adopts EDXACT' s tools

**GRENOBLE, France, March 12, 2007** – EDXACT SA today announced that its JIVARO netlist reduction tool was chosen by one of Japan's leading worldwide suppliers of semiconductor devices. According a three-year agreement, JIVARO will be integrated into the company's verification flow for high density IC designs.

EDXACT (Voiron, France) provides software solutions that help to accelerate the overall backend IC physical verification cycle. JIVARO innovative tools apply user-controllable model order reduction techniques upon huge parasitic data files obtained from layout extraction tools, before feeding them to simulation tools. Thanks to JIVARO, developers are now able to continue to use their existing simulation tools for new designs that otherwise would have been much too large. JIVARO's technology achieves dramatic speed improvements with maintained accuracy, which is mandatory for backend verification flows.

"This is our first inroad into the Japanese market, and we are looking forward for further success, thanks to the experience of Marubeni Solutions Corporation, our distributor in Japan." said Mathias Silvant, EDXACT President. "Our tools have now been chosen by companies in Europe, in the USA and in Asia, and they are integrated into verification flows for Soc design, memory design as well as processor design."

#### About EDXACT

Founded in 2004, EDXACT SA (Electronic Design: eXtraction, Analysis and Control Tools) focuses on electronic design tools aimed at physical verification tasks. EDXACT's innovative and patent pending model order reduction technology helps accelerate extensive simulations needed for backend verifications in complex mixed-signal IC design cycles. EDXACT's headquarters are based in Grenoble area, France. For additional information please visit EdXact online at [www.edxact.com](http://www.edxact.com) or send your questions to [info@edxact.com](mailto:info@edxact.com).

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