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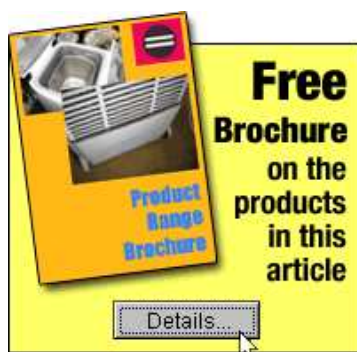
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Product category: **Design and Development Software**
 News Release from: [Edxact](#) | Subject: **Jivaro netlist reduction tool**
 Edited by the Electronicstalk Editorial Team on **9 November 2007**

Software helps verify A/D convertors



Jivaro tools apply user-controllable reduction techniques upon parasitic data files obtained from layout extraction tools

EdXact's Jivaro netlist reduction tool was chosen by e2v, a developer and manufacturer of specialised components and subsystems. e2v is using Jivaro to help verify its A/D convertors, developed using Jazz Semiconductor's SiGe BiCMOS 0.18-micron process. The new convertor family includes quad 8bit devices

capable of delivering conversion rates from 1.25 to 5GSps from a single chip at 1W per channel.

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EdXact provides software solutions that help to accelerate the overall backend IC physical verification cycle.

Jivaro tools apply user-controllable reduction techniques upon parasitic data files obtained from layout extraction tools.

This helps simulation tools to cope with huge data files while still maintaining accuracy.

Jivaro was chosen to help accelerate postlayout verifications on the A/D convertors' design. On that A/D mixed signal design, Jivaro-enabled simulations proved to execute three to 10 times faster, with the same level of accuracy, allowing more verifications to be executed and larger blocks to be verified, while still meeting tape-out delivery schedules.

Multiple simulation runs increase verification confidence, which is crucially important during the tape-out process.

Moreover, Jivaro's ease of use allows quick adoption of the tool by designers.

'Thanks to Jivaro, we were able to meet our just in time constraints and to increase our verification targets as well' according to D Boisgontier, manager of e2v's Broadband Data Convertor Development Team.

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