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Product category: **Design and Development Software**

News Release from: [Edxact](#) | Subject: **Jivaro HD and Comanche**

Edited by the Electronicstalk Editorial Team on **29 May 2007**

EDA tools target complexity at 65nm and below

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Upgraded netlist reduction and interconnect analysis tools help IC designers to optimise post-layout simulations, to maintain verification accuracy and to meet time to market goals

Edxact has released new versions of both its Jivaro

netlist reduction technology and its Comanche interconnection analysis tool. In addition to numerous additional features, capacity increase, support of inductance and mutual inductance in large files in custom flows and a graphical user interface into the Cadence Analog Environment are the major innovations.

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Version 4.0 of Jivaro HD (high density) and version 1.1 of Comanche will be demonstrated at the Design Automation Conference in San Diego, California, from 4th to 8th June 2007.

Edxact has enhanced its proprietary technology, allowing for a substantial increase in capacity for the products that are built using it, including Jivaro and Comanche.

These tools help IC designers to optimise post-layout simulations, to maintain verification accuracy and to meet time to market goals.

The Jivaro family of tools performs the reduction of parasitic files obtained from layout extraction tools, before feeding them to simulation tools, achieving dramatic speed improvements.

The 4.0 Release (dubbed HD for high density), increasing its capacity to several tens of gigabytes for nets with RLCK elements is a powerful tool when used with designs targeting 90 and 65nm geometries and below.

An accrued need for more detailed parasitics in design and post-layout verification comes along with those modern technologies.

Jivaro HD brings another capacity enhancement regarding the length of the nets that can be handled and the number of ports to one and the same net, as well as the number of parasitic elements accepted on the same net, which is dramatically increased.

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Edxact has joined a new category of members of the Connections Programme, called Emerging Solutions Members, which offer cutting-edge tools

Japanese success for netlist reduction tool

The Jivaro netlist reduction tool from Edxact has been chosen by one of Japan's leading worldwide suppliers of semiconductor devices

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[Software extends focus to IC-package codesign](#)

Software combines core switching, power delivery network, I/O subsystem and package/PCB models in a single environment for accurate

IC-package codesign

As a result, the tool is now able to perform outstanding remodelling of power nets.

Edxact has also extended the tool's capability to select parts of the netlist and to assign accuracy levels in order to optimise the tradeoffs between accuracy and simulation speedup.

'Model order reduction replaces the parasitic model by an equivalent model of smaller order', explains Corine Lamagdeleine, Edxact's Product Marketing Manager.

'Designers now can select accuracy levels based on the delay or frequency on a net'.

Along with an important increase in capacity, Comanche 1.1, the latest upgrade of Edxact's analysis tool to be showcased at DAC, is now able to compute S-parameter data between ports in high frequency circuits.

Outputs are in Touchstone compatible format, so that the designer can enhance its HF simulations with detailed S-parameters computed by Comanche.

By taking parasitic netlists and computing global values of interconnection resistance, impedance and delay, as well as S, Y and Z parameters for sets of ports, Comanche is a powerful analysis tool helping to rapidly pinpoint gross violations before simulation.

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