



News Release

EDXACT's JIVARO tools qualified by ST for post layout simulation flow

With this adoption, JIVARO improves the netlist reduction and simulation performance within STMicroelectronics's simulation tool suite.

GRENOBLE, France, July 24th, 2006 - EDXACT today announced that STMicroelectronics has added EDXACT's JIVARO parasitic reduction tools to its Post Layout Simulation flow (PLS), in order to speed up simulations of back-annotated netlists. JIVARO is a family of standalone reduction tools that remodel parasitics data obtained from layout extraction tools before feeding them to simulation tools. JIVARO's model order reduction techniques outstandingly reduce parasitic file size and data complexity while maintaining accuracy. ST has added JIVARO as postprocessor to the layout extractors used in some post layout analysis flows for transistor based design.

Supporting all major netlist formats like SPEF, DSPF, SPECTRE or SPICE, JIVARO enabled ST to standardize on one reduction engine for all extraction tools; which enhances interoperability and helps to save flow integration time. Moreover, unlike integrated reduction algorithms that often lead to undetermined accuracy, JIVARO gives designers the flexibility to accurately control speed-accuracy tradeoffs. JIVARO covers analog, RF, mixed-signal and digital designs and has been successfully used for various types of circuits.

"We did extensive testing on various designs and in different compression modes; it was very impressive that JIVARO allows accurate back-annotated simulations in a fraction of time we used before," said Jean-Paul Morin, Analog/RF CAD manager at STMicroelectronics. "EDXACT is focused on one of our major problems in IC design: exhaustive post-layout analysis with complete back-annotated parasitic data. With the help of EDXACT's team, JIVARO was successfully coupled on extraction tools we currently use, so we can expect important productivity gains and improved quality in our backend verification flow."

"We are pleased by STMicroelectronics's commitment", said Mathias Silvant, EDXACT President. "Parasitics from substrate, interconnects and package need to be taken into account in today's sign-off verifications in order to judge on the chance of silicon success and to reduce design cycles. The remodelling of those huge and complicated amounts of data can only be done efficiently by dedicated tools.

EDXACT's expertise spans on layout extraction and simulation for post layout verification and is dedicated on parasitic analysis techniques.

About EDXACT

Founded in March 2004, EdXact (Electronic Design: eXtraction, Analysis and Control Tools) specializes in parasitic extraction and physical verification. EdXact's innovative netlist reduction technology won the French national price of innovative companies in 2004. EdXact's headquarters are based in Grenoble area, France. For additional information please visit EdXact online at www.edxact.com.

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