



News Release

EdXact redefines speed/accuracy trade-offs in layout verification

New version of JIVARO improves parasitic files capacity, enforces control of accuracy and helps enhancing computers performances for reliable sign-off simulations

Grenoble, France, February 22, 2006 – EdXact, the innovative European verification company, today introduces version 2.2 of its standalone parasitic reduction tool JIVARO. JIVARO 2.2 now supports any flavor of the various formats used for representing parasitic data of wires in a chip, like SPEF, DSPF or SPICE; this means that its powerful reduction engines now can be coupled to any major layout extraction tool including Synopsys Star-RCXT, Cadence Assura-RCX, Mentor Calibre-XRC and others.

With nanometer geometries introducing new physical effects, and chip sizes climbing over 400M transistors, backend verification is now a major bottleneck in the design cycle, which prevents designers to meet their time - to - market goals. Files containing parasitics used in backannotated simulations are becoming excessively large; as detailed information is required for accurate sign-off analysis, this leads to prohibitive simulation times while iterations are still needed to fix detected failures. In order to speed up simulation existing reduction techniques embedded into the extraction tools try to optimize the files, but this is at the expense of sign-off accuracy. That's why more than 60 % of leading-edge designs fail due to parasitic effects. With silicon respins in the million-dollar range, this is no more acceptable. Using the right set of highly accurate, yet scalable tools is crucial in order to ensure the time-to-market, but even more important the time-to-volume.

EDXACT introduces the first set of standalone Model Order Reduction tools able to substantially reduce parasitics, while preserving accuracy; accuracy stays unusually high and the trade-offs speed-accuracy are tightly controlled. JIVARO tools cover analog, RF, mixed-signal and digital designs. They are unique due to their compromiseless handling of coupling capacitors, inductors and even mutual inductors. JIVARO tools plug naturally into all major postlayout verification flows. JIVARO tools have been successfully used for circuits with integrated spiral inductors, Analog-Digital Converters, Memory, VCO, LDO, power amplifiers, imaging and many others.

Simulation results with the reduced files show negligible differences with regular simulation results and stay within 5 % when high speed rate is chosen. Precision levels are user configurable.

The brand new versions introduced at DATE are still more optimized, open to any format and capable of handling huge files. JIVARO 2.2 was successfully used on a 300 000 transistors RAM, with an extracted parasitic file size of 650 Bytes. In normal (high precision) compression mode, simulation times with a major Fast-Spice simulation tool fell from 47 hours without JIVARO to 20 hours. Degrading the accuracy to 97% by choosing more aggressive reduction, the same circuit was simulated within 2 hours.

Partnerships to optimize computing needs

JIVARO 2.2 supports multithreading and computing clusters and has been largely optimized with respect to memory usage. Support of HP-UX has been added.

EdXact recently joined Mentor Graphics's OpenDoor program, which implements a mechanism to promote the development of interfaces between EDA software from different providers. This partnership ensures a tight integration of JIVARO tools within the Mentor Graphics design flow.

EdXact also joined the Developer & Solution Partner Program (DSPP) from Hewlett-Packard, giving access to porting and migration assistance on HP products, especially the HP-UX operating systems on risk processors.

JIVARO-A (for analog and RF designs) and JIVARO-D (for digital and mixed-signal circuits) are available on SunOS, HP-UX, and Linux platforms. Demonstrations will take place at Date, March 7th – 9th 2006, booth # F24.

About EdXact

Founded in March 2004, EdXact (Electronic Design: eXtraction, Analysis and Control Tools) specializes in parasitic extraction and physical verification. EdXact's innovative netlist reduction technology won the French national price of innovative companies in 2004. EdXact's headquarters are based in Grenoble area, France. The company has established sales offices in Germany, Israel and in the United States. For additional information please visit EdXact online at www.edxact.com or send your questions to info@edxact.com.

EdXact contact: Delphine Billon, Marketing Assistant info@edxact.com WWW.edxact.com EDXACT Parc Work Center - Bat A Route des Bois 38500 Voiron Tel. +33 (0)4 76 66 89 80 Fax. +33 (0)4 76 67 36 99	Press contact: Chantal Cochini Chantal.cochini@lops.fr Phone: + 33 142 71 30 93 Fax: + 33 142 71 19 49 Mob: + 33 622 98 03 80
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