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Methodology Shift: Adopting a Design for Manufacture Flow
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Description :

RFICs are becoming more complex, packing several functions and supporting multiple frequency bands and wireless standards. Modeling inductance in its intended (e.g. spiral) and parasitic forms is crucial for successful design. This is uniquely handled by Helic's VeloceRF™ tool, which rapidly models inductance across the chip and produces RLCK netlists. Netlist size and appropriateness for simulation is of concern, particularly for large-scale designs dominated by interconnect parasitics and mutual inductances. Fortunately, edXact's Jivaro™ tool can now dramatically reduce large netlists arising from RLCK extraction, slashing simulation time with minimal sacrifices in accuracy. In this paper we demonstrate how VeloceRF and Jivaro can be ideally combined in a fast, efficient and accurate RFIC design flow. A real-life circuit design is showcased.

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