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Startup puts team to work on the data explosion

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Santa Cruz, Calif. — It may be unusual for a 10-person R&D team to work for four EDA companies in succession, but that's happening in Grenoble, France, where engineers once associated with substrate extraction provider Snaketech have launched an IC design tool startup called Edxact SA.

The company is now beginning to ship Jivaro, which Edxact calls the first tool-independent offering dedicated to parasitic netlist reduction.

As they moved from one EDA company to another, the team members worked on extraction products. And that's what led to the idea for Jivaro, said Mathias Silvant, Edxact's co-founder and president.

"We'd been working on extraction for analog, RF and digital simulators, and there was always one major problem when working with customers," he said. "That was getting a hand on the data explosion. So we said to ourselves, 'There must be somebody who takes care of that, in a way that's accurate.' "

The outcome was Jivaro, which provides netlist reduction for many types of parasitic netlist elements, including resistance, capacitance, inductance and mutual inductance. It also handles capacitive coupling, and works for both flat and hierarchical netlists. Without reduction, these parasitics can overwhelm simulators with data, making run-times lengthy and limiting the amount of analysis IC designers can do.

Nothing comes easy, however, even with a track record. "In order to get funding from European VCs, you need more than a prototype," Silvant said. "You need a running product that can be commercialized, and you need happy customers." That's why Edxact took a year to raise about \$2.55 million in first-round venture funding.

The startup claims to have some unique model-order reduction technology, and that's what fuels Jivaro. Silvant claimed Jivaro is the only tool that can handle model-order reduction on inductive effects, including mutual inductance, and to have the most accurate reduction of capacitive coupling.

At last month's Design Automation Conference, Edxact demonstrated two versions of the product: Jivaro-A for analog designs and Jivaro-D for digital. Jivaro-D offers faster performance but doesn't provide reduction for inductance.

One challenge Edxact faces is getting the product in front of North American users. The company's recent DAC exhibit was a first attempt. "We found our first [U.S.] prospects, but we need to come by and do some evaluations and follow-up," Silvant said. Edxact plans to set up a U.S. office next year.

The need for Jivaro, said Silvant, stems from the "incredible" files that can result from parasitic extraction. "We saw one 20-Gbyte DSPF [detailed standard parasitic format] file for digital, and that's not the biggest one," he said. "No simulator can swallow this capacity."

Depending on the design, Jivaro promises to speed analysis times by as much as 100 times. It claims to work for any kind of simulator or timing analyzer. The reduction is even useful for "fast Spice" simulators, Silvant said.

Jivaro will fit into existing EDA tool flows, using inputs and outputs in standard formats such as DSPF, SPEF, Spice and Spectre, Silvant said. It supports multithreading and distributed processing.

Edxact's team was formed in the late '90s. Silvant said the team members were initially hired in 1998 and 1999 to work for Snaketech, which was subsequently acquired by Simplex Solutions. The entire team then moved to Simplex and ultimately to Cadence Design Systems when it acquired Simplex.

Then Cadence closed down its Grenoble research facility and laid off the entire team. "The team that was laid off in 2003 included management, applications engineers, R&D and everything, so we covered all the different aspects," said Silvant.

In March 2004, Silvant founded Edxact, along with co-founders Stephane Guedon, manager of R&D, and Frederic Giroud, manager of development and industrialization, and rehired the team.

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