

French Startup EdXact to Introduce Jivaro Twins

May 25, 2005 -- EdXact will introduce two versions of its standalone netlist reduction tool, Jivaro, at the Design Automation Conference (DAC) in Anaheim. Jivaro-A for analog and RF circuits, and Jivaro-D for digital and mixed-signal circuits, are netlist reduction tools that can handle accurately coupled capacitors, inductors and even mutual inductors. Both tools are standalone and complementary to all major EDA vendors' tools, plugging into existing flows through transparent interfaces based on SPICE, SPECTRE, DSPF and SPEF file formats.

According to the company, Jivaro is the first tool able to handle all types of parasitic netlist components: R, RC, RLC, RLCK, coupled, decoupled, inductance, mutual inductance and substrate. Jivaro netlist reduction technology uses no heuristics and relies on mathematically proven algorithms. This leads to up to 99% reduction of parasitic components and file size, but the main goal is to boost the simulators by assuring the accuracy. Memory consumption reduction and simulation speedups between 10x and 100x have been confirmed. "These results are now available for most existing tools, at the cost of a mere plug-in, " boasts Mathias Silvant, EdXact president."

Also, according to the company, Jivaro tools have been evaluated by several semiconductor industry leaders. For an RF circuit (LNA), DC simulation time dropped from 33 min to 6 s, leading to 330x speedup; S-parameter analysis time dropped from 1h 40 min to 9 s, an amazing 666-fold speedup. For a mixed-signal circuit (1 GHz ADC), transient spice simulation achieved a speed-up from 1 day to 5 hours. And a digital ring oscillator's transient simulation, first proving unable to reach convergence, achieved convergence and correct results with the same simulator after adding Jivaro into the flow.

Availability

Jivaro-A and Jivaro-D are available on Sun, Intel and HP platforms running Unix or Linux operating system.

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