

French startup EdXact to introduce JIVARO Twins at DAC

Tools fit seamlessly into existing digital and analog flows, providing efficient standalone model reduction for fast and accurate sign-off verification.

GRENOBLE, France, May 23, 2005 – EdXact, the innovative physical verification company, will introduce two versions of its standalone netlist reduction tool JIVARO, due for demonstration for the first time at the next DAC Conference in June in Anaheim. JIVARO-A for analog and RF circuits, and JIVARO-D for digital and mixed-signal circuits, are the first netlist reduction tools able to handle accurately coupled capacitors, inductors and even mutual inductors. Both tools are standalone and complementary to all major EDA vendors' tools, plugging into existing flows through transparent interfaces based on SPICE, SPECTRE, DSPF and SPEF file formats. This helps accelerating accurate post-layout verification necessary to reduce the number of re-spins, one of the biggest challenges in today's semiconductor industry.

With nanometer geometries, post-layout verification of complex ICs must take formerly negligible physical effects into account. An extracted netlist with backannotation of the required parasitic elements, necessary for accurate simulation, leads to a data explosion. This in turn drives the need for advanced parasitic reduction methods allowing a reasonable amount of data and still ensuring accuracy. JIVARO provides unparalleled netlist reduction capabilities and is the first tool able to handle all types of parasitic netlist components: R, RC, RLC, RLCK, coupled, decoupled, inductance, mutual inductance and substrate. JIVARO netlist reduction technology uses no heuristics and relies on mathematically proven algorithms. This leads to up to 99% reduction of parasitic components and file size, but the main goal is to boost the simulators by assuring the accuracy. Memory consumption reduction and simulation speedups between 10x and 100x have been confirmed. « These results are now available for most existing tools, at the cost of a mere plug-in, » stated Mathias Silvant, EdXact President. « Our JIVARO tools enable faster time-to-market through a reliable sign-off, easier analysis and the ability of full-chip simulation, » continued Silvant. Moreover, JIVARO is scalable, precision being controlled by the user with only one parameter.

JIVARO-A and JIVARO-D now offer proven support for more different flows, including analog, RF, mixed and digital. New features offer support for SPEF file format in addition of SPICE, DSPF and SPECTRE, as well as task parallelization and support for Linux clusters.

JIVARO tools have been evaluated by several semiconductor industry leaders. For an RF circuit (LNA), DC simulation time dropped from 33 min to 6 s, leading to 330x speedup; S-parameter analysis time dropped from 1h 40 min to 9 s, an amazing 666-fold speedup. For a mixed-signal circuit (1 GHz ADC), transient spice simulation achieved a speed-up from 1 day to 5 hours. And a digital ring oscillator's transient simulation, first proving unable to reach convergence, achieved convergence and correct results with the same simulator after adding JIVARO into the flow.

« I am impressed by the originality of the solution provided by EdXact, which enables drastic reductions of simulation times for complex sub-100-nm ICs, both digital and analog, » said Joseph Borel, formerly executive vice president for corporate EDA at STMicroelectronics, who recently joined the supervisory board of EdXact. « EdXact has a good sense of today's semiconductor industry's challenges, as attest further product developments, » concluded Borel.

JIVARO-A and JIVARO-D are available on Sun, Intel and HP platforms running Unix or Linux operating system. Demonstrations will take place at DAC in Anaheim, June 13-17, EdXact booth 357

About EdXact

Founded in March 2004 EdXact (Electronic Design eXtraction, Analysis and Control Tools) specializes in physical verification. EdXact's innovative technology won support from the French R&D ministry and from GRAIN (Grenoble Alpes Incubation.) Their first round of financing was raised in May 2005 from Emertec Gestion and I-Source Gestion, two funds specializing respectively in microelectronics and information technology infrastructures, and secured 2M Euros (2.6 M\$). EdXact's headquarters are based in Voreppe, near Grenoble, France, and the company is part of « Isère Entreprendre » group.

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